Universal performance counters unit

User manual
Version 3.0

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Introduction

This document describes hardware and software interfaces for the Universal Performance Counter (UPC) unit. The UPC allows for monitoring a set of selected hardware events generated by a variety of on-chip event sources such as the processors and floating point units, the snoop filters, the L2-caches, the L3-cache, and the network interfaces. Since the UPC is shared among all connected devices, its counters are flexibly configurable.

An overview of the architecture of BlueGene/P UPC is illustrated in Figure 1. The UPC unit contains 256 64-bit registers. All counters are configured individually using the configuration register associated to each counter. Each configuration register determines if the counter is counting level or edge sensitive events, if it has interrupt enabled to raise an interrupt when reaching a predetermined threshold value, and which of two events it is counting. There is one interrupt line coming out of the UPC module to indicate that any one of the counters has reached the threshold value. The single interrupt is fast and is on the boundary of 2^{12}. All counters and all configuration registers in the UPC module are mapped into the memory address space providing memory-mapped access to all counters and configuration register.

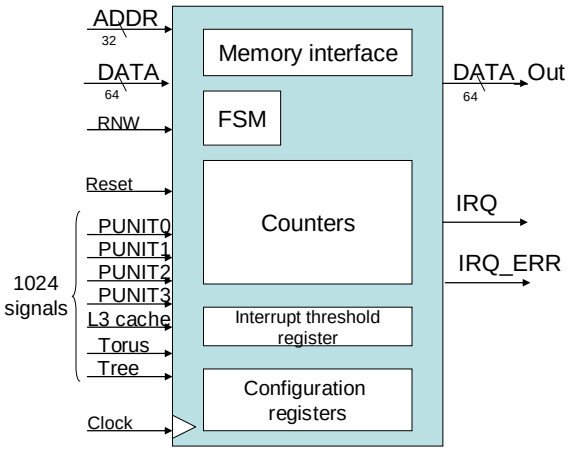

Figure 1: Universal performance counters block diagram

The design allows for multiple counters having interrupt enabled, but there is only one threshold register. Thus, interrupts can be enabled for several counters, but all these counters will check against the same threshold value.

The second interrupt line is an error indication interrupt and is asserted when one or more of error conditions are identified.

The UPC unit can assert two interrupt signals:

- IRQ - if a counter reaches the threshold value, and interrupt for that counter is enabled
- IRQ_err - if a parity error in counters is detected, if an improper bus request was made, or if a parity error on the address, data on the bus, or control signals was detected.

Counters are grouped into 32 identical counter groups, each group having eight counters. Each counter group is controlled by a single configuration register. Four configuration bits are used per counter to select counter mode, one of two inputs, and to enable interrupt. This is illustrated in figure 2.

To enable counting of fast events - events which are in the clock_x1 domain, such as L1 events - the UPC unit contains 72 fast counters. Remaining 184 counters count events which are in the clock_x2 domain (half processor frequency).

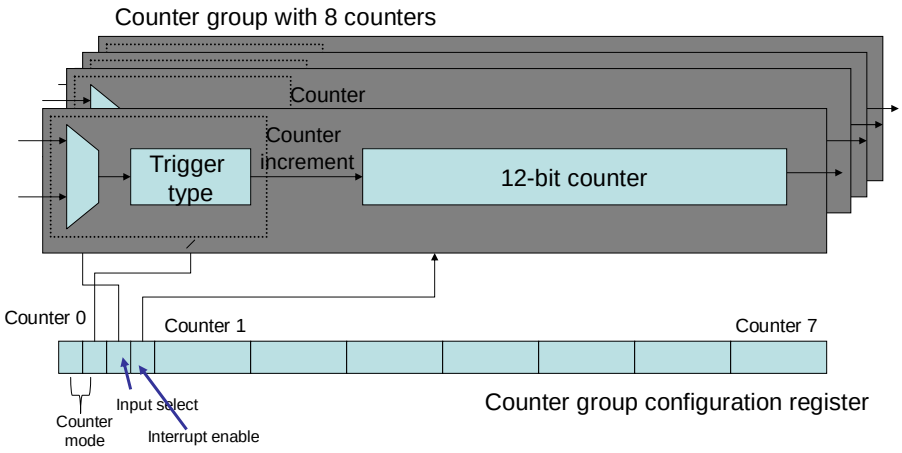

Figure 2: Counter group and counter group configuration register.

Group counter configuration registers

Overview

Groups of eight counters are grouped into a counter group which is controlled by a single configuration register. Each counter is configured using four configuration bits to define its characteristics, such as counter event, counter input, and interrupt enable.

The bits 0 to 3 control counter 0 in the group N, bits 4 to 7 counter 1, …, and bits 28 to 31 are for the counter 7 in the group N, as illustrated in Figure 2.

Two bits for counter events determine what signaling on the selected counter input represents a count-event. The user has the choice between level-sensitive events (low-/or high-active) and edge-sensitive signaling (low-high-/or high-low transition).

The encoding of counter events bits is as follows:

- 00 – high level sensitive
- 01 – low-high edge sensitive
- 10 – high-low edge sensitive
- 11 – low level sensitive

The counter input bit selects one of the two inputs per two mode groups:

- 0 – select input 0
- 1 – select input 1

The counters can be configured to select one of four input signals, enabling the total of 1024 events. All inputs are grouped into four user modes (0, 1, 2 and 3), each having 256 events. The user can select any input from the user modes 0 and 1, or from user modes 2 and 3. This selection is controlled with setting of the above bit.

However, the user can not intermix events from the modes 0-1, and 2-3. The selection if the user modes 0-1 or 2-3 are used is performed by the configuration and status register (CSR) bit 30. Setting CSR(30) to zero selects events from modes 0-1 are selected, otherwise events from modes 2-3 are counted.

Interrupt enable bit enables interrupt for this counter if it matches the threshold value:

- 0 – interrupt disabled
- 1 – interrupt enabled

Configuration and status register

The UPC unit can be programmed to count one of four events in four counter modes – 0, 1, 2 and 3. Every counter can be individually programmed to select events from either mode 0 and mode 1, or mode 2 and mode 3. Selection of mode (0&1) or (2&3) is done generally for the whole UPC unit. The counter event and interrupt setting is taken from the configuration register.

Additionally, all counters can be enabled and disabled simultaneously. This is controlled by setting the LSB of this register.

When IRQ_err signal is asserted, this register contains data parity bits of the latest bus write transfer which caused the interrupt, as well as the information if the address

parity caused interrupt, incorrect bus request or SRAM parity error. It is the responsibility of software to clear these bits during interrupt handling.

Bits 0-7 Input data parity bits
Bit 8 Address parity error
Bit 9 Bus error
Bit 10 SRAM parity error
Bit 11 Bus control parity error
Bits 12-29 unused
Bit 30 counter mode selection:

- 0 – select modes 0-1
- 1 – select modes 2-3

Bit 31 Enable/ disable all counters:

- 1 – enable
- 0- disable

Note that after the reset counters are disabled and have to be enabled by software by setting the Bit 31 of this register.

Resetting the counters

In Blue Gene/P architecture, the performance counters are implemented using the SRAM block for higher 52 bits. Thus, after turning the reset signal off, the value in higher 52 bits of the counters can be any arbitrary number. The counters do not need to be reset to zero to be able to use them – the user can read the values of counters before and after observed period. As counters will never overflow (or will overflow only once if random start value is very high) the exact number of counted events can always be determined.

The UPC unit supports writing of any arbitrary number to a counter. This can be used to pre-set the counters to desired value. This is especially useful if using threshold register and enabling the interrupt. For example, if the interrupt has to be raised for an event which will maybe occur only once or never, this can be implemented as follows:

- set threshold register to desired value (for example 0x0000BEEFDEADB000)
- set interrupt enable bit for the counter (for example counter 1_2)
- write the value decremented by one at the 12 bit boundary in the counter (in this example write the value 0x0000BEEFDEADAFFF in the counter 1_2).

When the observed event happens, the 12 bit counter will overflow causing the higher bits of the counter to be incremented. Comparison to the threshold register will fire the interrupt.

Memory address mapping

All counters, configuration registers, and the threshold register are memory mapped and are aligned on the 64 bit boundary.

All counters and registers can be written into and read out. Here is the short list of supported operations:

- write configuration register
- read configuration register
- write interrupt threshold register- atomic
- read interrupt threshold register – atomic
- write a counter – atomic
- read a counter - atomic

The UPC unit does not support writing bytes or half-words. Configuration registers are accessed using 32 bit wide load and store operations. For all 64 bit wide registers, i.e., the counters and the threshold register, 64b double load and store are used. On a counter read, 64 b wide data are read out.

Memory Map

Alias	Register Name	Memory Address	Value
Cnt0_0	Counter 0_0	0x710000000	Actual value of the counter 0-0
Cnt0_1	Counter 0_1	0x710000008	Actual value of the counter 0-1
Cnt0_2	Counter 0_2	0x710000010	Actual value of the counter 0-2
Cnt0_3	Counter 0_3	0x710000018	Actual value of the counter 0-3
Cnt0_4	Counter 0_4	0x710000020	Actual value of the counter 0-4
Cnt0_5	Counter 0_5	0x710000028	Actual value of the counter 0-5
Cnt0_6	Counter 0_6	0x710000030	Actual value of the counter 0-6
Cnt0_7	Counter 0_7	0x710000038	Actual value of the counter 0-7
Cnt1_0	Counter 1_0	0x710000040	Actual value of the counter 1-0
Cnt1_1	Counter 1_1	0x710000048	Actual value of the counter 1-1
Cnt1_2	Counter 1_2	0x710000050	Actual value of the counter 1-2
Cnt1_3	Counter 1_3	0x710000058	Actual value of the counter 1-3
Cnt1_4	Counter 1_4	0x710000060	Actual value of the counter 1-4
Cnt1_5	Counter 1_5	0x710000068	Actual value of the counter 1-5
Cnt1_6	Counter 1_6	0x710000070	Actual value of the counter 1-6
Cnt1_7	Counter 1_7	0x710000078	Actual value of the counter 1-7
	. . .		
Cnt31_0	Counter 31_0	0x7100007C0	Actual value of the counter 31_0
Cnt31_1	Counter 31_1	0x7100007C8	Actual value of the counter 31_1
Cnt31_2	Counter 31_2	0x7100007D0	Actual value of the counter 31_2
Cnt31_3	Counter 31_3	0x7100007D8	Actual value of the counter 31_3
Cnt31_4	Counter 31_4	0x7100007E0	Actual value of the counter 31_4
Cnt31_5	Counter 31_5	0x7100007E8	Actual value of the counter 31_5
Cnt31_6	Counter 31_6	0x7100007F0	Actual value of the counter 31_6
Cnt31_7	Counter 31_7	0x7100007F8	Actual value of the counter 31_7

GCR0	Group Configuration	0x710000800	Counter-Group-0 configuration register
GCR1	Group Configuration	0x710000808	Counter-Group-1 configuration register
	. . .		
GCR31	Group Configuration	0x7100008F8	Counter-Group-31 configuration register
CSR	Configuration & status register	0x710000910	CSD(30) selects counting events from Mode 0&1 or Mode 2&3 CSR(31) enables/disables counters
PEA	Address causing parity error	0x710000918	Stored the address on the bus for which address or data byte parity error is detected
TRR	Threshold	0x710000FF8	Interrupt threshold register

Event mapping

This chapter lists the mapping of events for each counter and configuration bits required to select this event. The meaning of each event signal is given in the following chapters.

No. - event number
Cnt - counter
CD - clock domain (1 for processor frequency, 0 for ½ processor frequency)
UM - user mode 0, 1, 2 & 3
CSR(30) - value of the bit 30 in the configuration status register
CRA - address of the configuration register
BCR - Bit offset of the configuration register which controls this event selection
VBCR - value of the bit BCR in the configuration register ACR to select this event

No.	Counter number	Event	Counter address	Cnt	CD	UM	CSR (30)	CRA	BCR	VB CR
0	0	Dp0-pp0(0)	0x710000000	0-0	1	0	0	0x710000800	2	0
1	0	Dp1_pp0(0)	0x710000000	0-0	1	1	0	0x710000800	2	1
2	1	Dp0-pp0(1)	0x710000008	0-1	1	0	0	0x710000800	6	0
3	1	Dp1_pp0(1)	0x710000008	0-1	1	1	0	0x710000800	6	1
4	2	Dp0-pp0(2)	0x710000010	0-2	1	0	0	0x710000800	10	0
5	2	Dp1_pp0(2)	0x710000010	0-2	1	1	0	0x710000800	10	1
6	3	Dp0-pp0(3)	0x710000018	0-3	1	0	0	0x710000800	14	0
7	3	Dp1_pp0(3)	0x710000018	0-3	1	1	0	0x710000800	14	1
8	4	Dp0-pp0(4)	0x710000020	0-4	1	0	0	0x710000800	18	0
9	4	Dp1_pp0(4)	0x710000020	0-4	1	1	0	0x710000800	18	1
10	5	Dp0-pp0(5)	0x710000028	0-5	1	0	0	0x710000800	22	0
11	5	Dp1_pp0(5)	0x710000028	0-5	1	1	0	0x710000800	22	1
12	6	Dp0-pp0(6)	0x710000030	0-6	1	0	0	0x710000800	26	0
13	6	Dp1_pp0(6)	0x710000030	0-6	1	1	0	0x710000800	26	1
14	7	Dp0-pp0(7)	0x710000038	0-7	1	0	0	0x710000800	30	0
15	7	Dp1_pp0(7)	0x710000038	0-7	1	1	0	0x710000800	30	1
16	8	Dp0-pp0(8)	0x710000040	1-0	1	0	0	0x710000808	2	0
17	8	Dp1_pp0(8)	0x710000040	1-0	1	1	0	0x710000808	2	1
18	9	Dp0-pp0(9)	0x710000048	1-1	1	0	0	0x710000808	6	0
19	9	Dp1_pp0(9)	0x710000048	1-1	1	1	0	0x710000808	6	1
20	10	Dp0-pp0(10)	0x710000050	1-2	1	0	0	0x710000808	10	0
21	10	Dp1_pp0(10)	0x710000050	1-2	1	1	0	0x710000808	10	1
22	11	Dp0-pp0(11)	0x710000058	1-3	1	0	0	0x710000808	14	0
23	11	Dp1_pp0(11)	0x710000058	1-3	1	1	0	0x710000808	14	1
24	12	Dp0-pp0(12)	0x710000060	1-4	1	0	0	0x710000808	18	0
25	12	Dp1_pp0(12)	0x710000060	1-4	1	1	0	0x710000808	18	1
26	13	Dp0-pp0(13)	0x710000068	1-5	1	0	0	0x710000808	22	0
27	13	Dp1_pp0(13)	0x710000068	1-5	1	1	0	0x710000808	22	1
28	14	Dp0-pp0(14)	0x710000070	1-6	1	0	0	0x710000808	26	0
29	14	Dp1_pp0(14)	0x710000070	1-6	1	1	0	0x710000808	26	1
30	15	Dp0-pp0(15)	0x710000078	1-7	1	0	0	0x710000808	30	0
31	15	Dp1_pp0(15)	0x710000078	1-7	1	1	0	0x710000808	30	1
32	16	Dp0-pp0(16)	0x710000080	2-0	1	0	0	0x710000810	2	0
33	16	Dp1_pp0(16)	0x710000080	2-0	1	1	0	0x710000810	2	1

34	17	Dp0-pp0(17)	0x710000088	2-1	1	0	0	0x710000810	6	0
35	17	Dp1_pp0(17)	0x710000088	2-1	1	1	0	0x710000810	6	1
36	18	Dp0-pp0(18)	0x710000090	2-2	1	0	0	0x710000810	10	0
37	18	Dp1_pp0(18)	0x710000090	2-2	1	1	0	0x710000810	10	1
38	19	Dp0-pp0(19)	0x710000098	2-3	1	0	0	0x710000810	14	0
39	19	Dp1_pp0(19)	0x710000098	2-3	1	1	0	0x710000810	14	1
40	20	Dp0-pp0(20)	0x7100000a0	2-4	1	0	0	0x710000810	18	0
41	20	Dp1_pp0(20)	0x7100000a0	2-4	1	1	0	0x710000810	18	1
42	21	Dp0-pp0(21)	0x7100000a8	2-5	1	0	0	0x710000810	22	0
43	21	Dp1_pp0(21)	0x7100000a8	2-5	1	1	0	0x710000810	22	1
44	22	Dp0-pp0(22)	0x7100000b0	2-6	1	0	0	0x710000810	26	0
45	22	Dp1_pp0(22)	0x7100000b0	2-6	1	1	0	0x710000810	26	1
46	23	Dp0-pp0(23)	0x7100000b8	2-7	1	0	0	0x710000810	30	0
47	23	Dp1_pp0(23)	0x7100000b8	2-7	1	1	0	0x710000810	30	1
48	24	Dp0-pp0(24)	0x7100000c0	3-0	1	0	0	0x710000818	2	0
49	24	Dp1_pp0(24)	0x7100000c0	3-0	1	1	0	0x710000818	2	1
50	25	Dp0-pp0(25)	0x7100000c8	3-1	1	0	0	0x710000818	6	0
51	25	Dp1_pp0(25)	0x7100000c8	3-1	1	1	0	0x710000818	6	1
52	26	Dp0-pp0(26)	0x7100000d0	3-2	1	0	0	0x710000818	10	0
53	26	Dp1_pp0(26)	0x7100000d0	3-2	1	1	0	0x710000818	10	1
54	27	Dp0-pp0(27)	0x7100000d8	3-3	1	0	0	0x710000818	14	0
55	27	Dp1_pp0(27)	0x7100000d8	3-3	1	1	0	0x710000818	14	1
56	28	Dp0-pp0(28)	0x7100000e0	3-4	1	0	0	0x710000818	18	0
57	28	Dp1_pp0(28)	0x7100000e0	3-4	1	1	0	0x710000818	18	1
58	29	Dp0-pp0(29)	0x7100000e8	3-5	1	0	0	0x710000818	22	0
59	29	Dp1_pp0(29)	0x7100000e8	3-5	1	1	0	0x710000818	22	1
60	30	Dp0-pp0(30)	0x7100000f0	3-6	1	0	0	0x710000818	26	0
61	30	Dp1_pp0(30)	0x7100000f0	3-6	1	1	0	0x710000818	26	1
62	31	Dp0-pp0(31)	0x7100000f8	3-7	1	0	0	0x710000818	30	0
63	31	Dp1_pp0(31)	0x7100000f0	3-7	1	1	0	0x710000818	30	1
64	32	Dp0-pp0(32)	0x710000100	4-0	1	0	0	0x710000820	2	0
65	32	Dp1_pp0(32)	0x710000100	4-0	1	1	0	0x710000820	2	1
66	33	Dp0-pp0(33)	0x710000108	4-1	1	0	0	0x710000820	6	0
67	33	Dp1_pp0(33)	0x710000108	4-1	1	1	0	0x710000820	6	1
68	34	Dp0-pp0(34)	0x710000110	4-2	1	0	0	0x710000820	10	0
69	34	Dp1_pp0(34)	0x710000110	4-2	1	1	0	0x710000820	10	1
70	35	Dp0-pp1(0)	0x710000118	4-3	1	0	0	0x710000820	14	0
71	35	Dp1-pp1(0)	0x710000118	4-3	1	1	0	0x710000820	14	1
72	36	Dp0-pp1(1)	0x710000120	4-4	1	0	0	0x710000820	18	0
73	36	Dp1-pp1(1)	0x710000120	4-4	1	1	0	0x710000820	18	1
74	37	Dp0-pp1(2)	0x710000128	4-5	1	0	0	0x710000820	22	0
75	37	Dp1-pp1(2)	0x710000128	4-5	1	1	0	0x710000820	22	1
76	38	Dp0-pp1(3)	0x710000130	4-6	1	0	0	0x710000820	26	0
77	38	Dp1-pp1(3)	0x710000130	4-6	1	1	0	0x710000820	26	1
78	39	Dp0-pp1(4)	0x710000138	4-7	1	0	0	0x710000820	30	0
79	39	Dp1-pp1(4)	0x710000138	4-7	1	1	0	0x710000820	30	1
80	40	Dp0-pp1(5)	0x710000140	5-0	1	0	0	0x710000828	2	0
81	40	Dp1-pp1(5)	0x710000140	5-0	1	1	0	0x710000828	2	1
82	41	Dp0-pp1(6)	0x710000148	5-1	1	0	0	0x710000828	6	0
83	41	Dp1-pp1(6)	0x710000148	5-1	1	1	0	0x710000828	6	1
84	42	Dp0-pp1(7)	0x710000150	5-2	1	0	0	0x710000828	10	0
85	42	Dp1-pp1(7)	0x710000150	5-2	1	1	0	0x710000828	10	1
86	43	Dp0-pp1(8)	0x710000158	5-3	1	0	0	0x710000828	14	0

87	43	Dp1-pp1(8)	0x710000158	5-3	1	1	0	0x710000828	14	1
88	44	Dp0-pp1(9)	0x710000160	5-4	1	0	0	0x710000828	18	0
89	44	Dp1-pp1(9)	0x710000160	5-4	1	1	0	0x710000828	18	1
90	45	Dp0-pp1(10)	0x710000168	5-5	1	0	0	0x710000828	22	0
91	45	Dp1-pp1(10)	0x710000168	5-5	1	1	0	0x710000828	22	1
92	46	Dp0-pp1(11)	0x710000170	5-6	1	0	0	0x710000828	26	0
93	46	Dp1-pp1(11)	0x710000170	5-6	1	1	0	0x710000828	26	1
94	47	Dp0-pp1(12)	0x710000178	5-7	1	0	0	0x710000828	30	0
95	47	Dp1-pp1(12)	0x710000178	5-7	1	1	0	0x710000828	30	1
96	48	Dp0-pp1(13)	0x710000180	6-0	1	0	0	0x710000830	2	0
97	48	Dp1-pp1(13)	0x710000180	6-0	1	1	0	0x710000830	2	1
98	49	Dp0-pp1(14)	0x710000188	6-1	1	0	0	0x710000830	6	0
99	49	Dp1-pp1(14)	0x710000188	6-1	1	1	0	0x710000830	6	1
100	50	Dp0-pp1(15)	0x710000190	6-2	1	0	0	0x710000830	10	0
101	50	Dp1-pp1(15)	0x710000190	6-2	1	1	0	0x710000830	10	1
102	51	Dp0-pp1(16)	0x710000198	6-3	1	0	0	0x710000830	14	0
103	51	Dp1-pp1(16)	0x710000198	6-3	1	1	0	0x710000830	14	1
104	52	Dp0-pp1(17)	0x7100001a0	6-4	1	0	0	0x710000830	18	0
105	52	Dp1-pp1(17)	0x7100001a0	6-4	1	1	0	0x710000830	18	1
106	53	Dp0-pp1(18)	0x7100001a8	6-5	1	0	0	0x710000830	22	0
107	53	Dp1-pp1(18)	0x7100001a8	6-5	1	1	0	0x710000830	22	1
108	54	Dp0-pp1(19)	0x7100001b0	6-6	1	0	0	0x710000830	26	0
109	54	Dp1-pp1(19)	0x7100001b0	6-6	1	1	0	0x710000830	26	1
110	55	Dp0-pp1(20)	0x7100001b8	6-7	1	0	0	0x710000830	30	0
111	55	Dp1-pp1(20)	0x7100001b8	6-7	1	1	0	0x710000830	30	1
112	56	Dp0-pp1(21)	0x7100001c0	7-0	1	0	0	0x710000838	2	0
113	56	Dp1-pp1(21)	0x7100001c0	7-0	1	1	0	0x710000838	2	1
114	57	Dp0-pp1(22)	0x7100001c8	7-1	1	0	0	0x710000838	6	0
115	57	Dp1-pp1(22)	0x7100001c8	7-1	1	1	0	0x710000838	6	1
116	58	Dp0-pp1(23)	0x7100001d0	7-2	1	0	0	0x710000838	10	0
117	58	Dp1-pp1(23)	0x7100001d0	7-2	1	1	0	0x710000838	10	1
118	59	Dp0-pp1(24)	0x7100001d8	7-3	1	0	0	0x710000838	14	0
119	59	Dp1-pp1(24)	0x7100001d8	7-3	1	1	0	0x710000838	14	1
120	60	Dp0-pp1(25)	0x7100001e0	7-4	1	0	0	0x710000838	18	0
121	60	Dp1-pp1(25)	0x7100001e0	7-4	1	1	0	0x710000838	18	1
122	61	Dp0-pp1(26)	0x7100001e8	7-5	1	0	0	0x710000838	22	0
123	61	Dp1-pp1(26)	0x7100001e8	7-5	1	1	0	0x710000838	22	1
124	62	Dp0-pp1(27)	0x7100001f0	7-6	1	0	0	0x710000838	26	0
125	62	Dp1-pp1(27)	0x7100001f0	7-6	1	1	0	0x710000838	26	1
126	63	Dp0-pp1(28)	0x7100001f8	7-7	1	0	0	0x710000838	30	0
127	63	Dp1-pp1(28)	0x7100001f8	7-7	1	1	0	0x710000838	30	1
128	64	Dp0-pp1(29)	0x710000200	8-0	1	0	0	0x710000840	2	0
129	64	Dp1-pp1(29)	0x710000200	8-0	1	1	0	0x710000840	2	1
130	65	Dp0-pp1(30)	0x710000208	8-1	1	0	0	0x710000840	6	0
131	65	Dp1-pp1(30)	0x710000208	8-1	1	1	0	0x710000840	6	1
132	66	Dp0-pp1(31)	0x710000210	8-2	1	0	0	0x710000840	10	0
133	66	Dp1-pp1(31)	0x710000210	8-2	1	1	0	0x710000840	10	1
134	67	Dp0-pp1(32)	0x710000218	8-3	1	0	0	0x710000840	14	0
135	67	Dp1-pp1(32)	0x710000218	8-3	1	1	0	0x710000840	14	1
136	68	Dp0-pp1(33)	0x710000220	8-4	1	0	0	0x710000840	18	0
137	68	Dp1-pp1(33)	0x710000220	8-4	1	1	0	0x710000840	18	1
138	69	Dp0-pp1(34)	0x710000228	8-5	1	0	0	0x710000840	22	0
139	69	Dp1-pp1(34)	0x710000228	8-5	1	1	0	0x710000840	22	1

140	70	Dp0-snp0(0)	0x710000230	8-6	1	0	0	0x710000840	26	0
141	70	Dp1-snp0(0)	0x710000230	8-6	1	1	0	0x710000840	26	1
142	71	Dp0-snp1(0)	0x710000238	8-7	1	0	0	0x710000840	30	0
143	71	Dp1-snp1(0)	0x710000238	8-7	1	1	0	0x710000840	30	1
144	72	Dp0-l20(0)	0x710000240	9-0	2	0	0	0x710000848	2	0
145	72	Tr_m1(0)	0x710000240	9-0	2	1	0	0x710000848	2	1
146	73	Dp0-l20(1)	0x710000248	9-1	2	0	0	0x710000848	6	0
147	73	Tr_m1(1)	0x710000248	9-1	2	1	0	0x710000848	6	1
148	74	Dp0-l20(2)	0x710000250	9-2	2	0	0	0x710000848	10	0
149	74	Tr_m1(2)	0x710000250	9-2	2	1	0	0x710000848	10	1
150	75	Dp0-l20(3)	0x710000258	9-3	2	0	0	0x710000848	14	0
151	75	Tr_m1(3)	0x710000258	9-3	2	1	0	0x710000848	14	1
152	76	Dp0-l20(4)	0x710000260	9-4	2	0	0	0x710000848	18	0
153	76	Tr_m1(4)	0x710000260	9-4	2	1	0	0x710000848	18	1
154	77	Dp0-l20(5)	0x710000266	9-5	2	0	0	0x710000848	22	0
155	77	Tr_m1(5)	0x710000266	9-5	2	1	0	0x710000848	22	1
156	78	Dp0-l20(6)	0x710000270	9-6	2	0	0	0x710000848	26	0
157	78	Tr_m1(6)	0x710000270	9-6	2	1	0	0x710000848	26	1
158	79	Dp0-l20(7)	0x710000278	9-7	2	0	0	0x710000848	30	0
159	79	Tr_m1(7)	0x710000278	9-7	2	1	0	0x710000848	30	1
160	80	Dp0-l20(8)	0x710000280	10-0	2	0	0	0x710000850	2	0
161	80	Tr_m1(8)	0x710000280	10-0	2	1	0	0x710000850	2	1
162	81	Dp0-l20(9)	0x710000288	10-1	2	0	0	0x710000850	6	0
163	81	Tr_m1(9)	0x710000288	10-1	2	1	0	0x710000850	6	1
164	82	Dp0-l20(10)	0x710000290	10-2	2	0	0	0x710000850	10	0
165	82	Tr_m1(10)	0x710000290	10-2	2	1	0	0x710000850	10	1
166	83	Dp0-l20(11)	0x710000298	10-3	2	0	0	0x710000850	14	0
167	83	Tr_m1(11)	0x710000298	10-3	2	1	0	0x710000850	14	1
168	84	Dp0-l20(12)	0x7100002a0	10-4	2	0	0	0x710000850	18	0
169	84	Tr_m1(12)	0x7100002a0	10-4	2	1	0	0x710000850	18	1
170	85	Dp0-l20(13)	0x7100002a8	10-5	2	0	0	0x710000850	22	0
171	85	Tr_m1(13)	0x7100002a8	10-5	2	1	0	0x710000850	22	1
172	86	Dp0-l20(14)	0x7100002b0	10-6	2	0	0	0x710000850	26	0
173	86	Tr_m1(14)	0x7100002b0	10-6	2	1	0	0x710000850	26	1
174	87	Dp0-l20(15)	0x7100002b8	10-7	2	0	0	0x710000850	30	0
175	87	Tr_m1(15)	0x7100002b8	10-7	2	1	0	0x710000850	30	1
176	88	Dp0-l20(16)	0x7100002c0	11-0	2	0	0	0x710000858	2	0
177	88	Tr_m1(16)	0x7100002c0	11-0	2	1	0	0x710000858	2	1
178	89	Dp0-l20(17)	0x7100002c8	11-1	2	0	0	0x710000858	6	0
179	89	Tr_m1(17)	0x7100002c8	11-1	2	1	0	0x710000858	6	1
180	90	Dp0-l20(18)	0x7100002d0	11-2	2	0	0	0x710000858	10	0
181	90	Tr_m1(18)	0x7100002d0	11-2	2	1	0	0x710000858	10	1
182	91	Dp0-l20(19)	0x7100002d8	11-3	2	0	0	0x710000858	14	0
183	91	Tr_m1(19)	0x7100002d8	11-3	2	1	0	0x710000858	14	1
184	92	Dp0-l20(20)	0x7100002e0	11-4	2	0	0	0x710000858	18	0
185	92	Tr_m1(20)	0x7100002e0	11-4	2	1	0	0x710000858	18	1
186	93	Dp0-l20(21)	0x7100002e8	11-5	2	0	0	0x710000858	22	0
187	93	Tr_m1(21)	0x7100002e8	11-5	2	1	0	0x710000858	22	1
188	94	Dp0-l20(22)	0x7100002f0	11-6	2	0	0	0x710000858	26	0
189	94	Tr_m1(22)	0x7100002f0	11-6	2	1	0	0x710000858	26	1
190	95	Dp0-l20(23)	0x7100002f8	11-7	2	0	0	0x710000858	30	0
191	95	Tr_m1(23)	0x7100002f8	11-7	2	1	0	0x710000858	30	1
192	96	Dp0-l20(24)	0x710000300	12-0	2	0	0	0x710000860	2	0

193	96	Tr_m1(24)	0x710000300	12-0	2	1	0	0x710000860	2	1
194	97	Dp0-l20(25)	0x710000308	12-1	2	0	0	0x710000860	6	0
195	97	Tr_m1(25)	0x710000308	12-1	2	1	0	0x710000860	6	1
196	98	Dp0-l20(26)	0x710000310	12-2	2	0	0	0x710000860	10	0
197	98	Tr_m1(26)	0x710000310	12-2	2	1	0	0x710000860	10	1
198	99	Dp0-l20(27)	0x710000318	12-3	2	0	0	0x710000860	14	0
199	99	Tr_m1(27)	0x710000318	12-3	2	1	0	0x710000860	14	1
200	100	Dp0-l20(28)	0x710000320	12-4	2	0	0	0x710000860	18	0
201	100	Tr_m1(28)	0x710000320	12-4	2	1	0	0x710000860	18	1
202	101	Dp0-l20(29)	0x710000328	12-5	2	0	0	0x710000860	22	0
203	101	Tr_m1(29)	0x710000328	12-5	2	1	0	0x710000860	22	1
204	102	Dp0-l20(30)	0x710000330	12-6	2	0	0	0x710000860	26	0
205	102	Tr_m1(30)	0x710000330	12-6	2	1	0	0x710000860	26	1
206	103	Dp0-l20(31)	0x710000338	12-7	2	0	0	0x710000860	30	0
207	103	Tr_m1(31)	0x710000338	12-7	2	1	0	0x710000860	30	1
208	104	Dp0-l21(0)	0x710000340	13-0	2	0	0	0x710000868	2	0
209	104	Tr_m1(32)	0x710000340	13-0	2	1	0	0x710000868	2	1
210	105	Dp0-l21(1)	0x710000348	13-1	2	0	0	0x710000868	6	0
211	105	Tr_m1(33)	0x710000348	13-1	2	1	0	0x710000868	6	1
212	106	Dp0-l21(2)	0x710000350	13-2	2	0	0	0x710000868	10	0
213	106	Tr_m1(34)	0x710000350	13-2	2	1	0	0x710000868	10	1
214	107	Dp0-l21(3)	0x710000358	13-3	2	0	0	0x710000868	14	0
215	107	Tr_m1(35)	0x710000358	13-3	2	1	0	0x710000868	14	1
216	108	Dp0-l21(4)	0x710000360	13-4	2	0	0	0x710000868	18	0
217	108	Tr_m1(36)	0x710000360	13-4	2	1	0	0x710000868	18	1
218	109	Dp0-l21(5)	0x710000368	13-5	2	0	0	0x710000868	22	0
219	109	Tr_m1(37)	0x710000368	13-5	2	1	0	0x710000868	22	1
220	110	Dp0-l21(6)	0x710000370	13-6	2	0	0	0x710000868	26	0
221	110	Tr_m1(38)	0x710000370	13-6	2	1	0	0x710000868	26	1
222	111	Dp0-l21(7)	0x710000378	13-7	2	0	0	0x710000868	30	0
223	111	Tr_m1(39)	0x710000378	13-7	2	1	0	0x710000868	30	1
224	112	Dp0-l21(8)	0x710000380	14-0	2	0	0	0x710000870	2	0
225	112	Tr_m1(40)	0x710000380	14-0	2	1	0	0x710000870	2	1
226	113	Dp0-l21(9)	0x710000388	14-1	2	0	0	0x710000870	6	0
227	113	Tr_m1(41)	0x710000388	14-1	2	1	0	0x710000870	6	1
228	114	Dp0-l21(10)	0x710000390	14-2	2	0	0	0x710000870	10	0
229	114	Tr_m1(42)	0x710000390	14-2	2	1	0	0x710000870	10	1
230	115	Dp0-l21(11)	0x710000398	14-3	2	0	0	0x710000870	14	0
231	115	Tr_m1(43)	0x710000398	14-3	2	1	0	0x710000870	14	1
232	116	Dp0-l21(12)	0x7100003a0	14-4	2	0	0	0x710000870	18	0
233	116	Tr_m1(44)	0x7100003a0	14-4	2	1	0	0x710000870	18	1
234	117	Dp0-l21(13)	0x7100003a8	14-5	2	0	0	0x710000870	22	0
235	117	Tr_m1(45)	0x7100003a8	14-5	2	1	0	0x710000870	22	1
236	118	Dp0-l21(14)	0x7100003b0	14-6	2	0	0	0x710000870	26	0
237	118	Tr_m1(46)	0x7100003b0	14-6	2	1	0	0x710000870	26	1
238	119	Dp0-l21(15)	0x7100003b8	14-7	2	0	0	0x710000870	30	0
239	119	Tr_m1(47)	0x7100003b8	14-7	2	1	0	0x710000870	30	1
240	120	Dp0-l21(16)	0x7100003c0	15-0	2	0	0	0x710000878	2	0
241	120	Tr_m1(48)	0x7100003c0	15-0	2	1	0	0x710000878	2	1
242	121	Dp0-l21(17)	0x7100003c8	15-1	2	0	0	0x710000878	6	0
243	121	Tr_m1(49)	0x7100003c8	15-1	2	1	0	0x710000878	6	1
244	122	Dp0-l21(18)	0x7100003d0	15-2	2	0	0	0x710000878	10	0
245	122	Tr_m1(50)	0x7100003d0	15-2	2	1	0	0x710000878	10	1

246	123	Dp0-l21(19)	0x7100003d8	15-3	2	0	0	0x710000878	14	0
247	123	Tr_m1(51)	0x7100003d8	15-3	2	1	0	0x710000878	14	1
248	124	Dp0-l21(20)	0x7100003e0	15-4	2	0	0	0x710000878	18	0
249	124	Tr_m1(52)	0x7100003e0	15-4	2	1	0	0x710000878	18	1
250	125	Dp0-l21(21)	0x7100003e8	15-5	2	0	0	0x710000878	22	0
251	125	Tr_m1(53)	0x7100003e8	15-5	2	1	0	0x710000878	22	1
252	126	Dp0-l21(22)	0x7100003f0	15-6	2	0	0	0x710000878	26	0
253	126	Tr_m1(54)	0x7100003f0	15-6	2	1	0	0x710000878	26	1
254	127	Dp0-l21(23)	0x7100003f8	15-7	2	0	0	0x710000878	30	0
255	127	Tr_m1(55)	0x7100003f8	15-7	2	1	0	0x710000878	30	1
256	128	Dp0-l21(24)	0x710000400	16-0	2	0	0	0x710000880	2	0
257	128	Tr_m1(56)	0x710000400	16-0	2	1	0	0x710000880	2	1
258	129	Dp0-l21(25)	0x710000408	16-1	2	0	0	0x710000880	6	0
259	129	Tr_m1(57)	0x710000408	16-1	2	1	0	0x710000880	6	1
260	130	Dp0-l21(26)	0x710000410	16-2	2	0	0	0x710000880	10	0
261	130	Tr_m1(58)	0x710000410	16-2	2	1	0	0x710000880	10	1
262	131	Dp0-l21(27)	0x710000418	16-3	2	0	0	0x710000880	14	0
263	131	Tr_m1(59)	0x710000418	16-3	2	1	0	0x710000880	14	1
264	132	Dp0-l21(28)	0x710000420	16-4	2	0	0	0x710000880	18	0
265	132	Dp1_l20(0)	0x710000420	16-4	2	1	0	0x710000880	18	1
266	133	Dp0-l21(29)	0x710000428	16-5	2	0	0	0x710000880	22	0
267	133	Dp1_l20(1)	0x710000428	16-5	2	1	0	0x710000880	22	1
268	134	Dp0-l21(30)	0x710000430	16-6	2	0	0	0x710000880	26	0
269	134	Dp1_l20(2)	0x710000430	16-6	2	1	0	0x710000880	26	1
270	135	Dp0-l21(31)	0x710000438	16-7	2	0	0	0x710000880	30	0
271	135	Dp1_l20(3)	0x710000438	16-7	2	1	0	0x710000880	30	1
272	136	L30-m0(0)	0x710000440	17-0	2	0	0	0x710000888	2	0
273	136	Dp1_l20(4)	0x710000440	17-0	2	1	0	0x710000888	2	1
274	137	L30-m0(1)	0x710000448	17-1	2	0	0	0x710000888	6	0
275	137	Dp1_l20(5)	0x710000448	17-1	2	1	0	0x710000888	6	1
276	138	L30-m0(2)	0x710000450	17-2	2	0	0	0x710000888	10	0
277	138	Dp1_l20(6)	0x710000450	17-2	2	1	0	0x710000888	10	1
278	139	L30-m0(3)	0x710000458	17-3	2	0	0	0x710000888	14	0
279	139	Dp1_l20(7)	0x710000458	17-3	2	1	0	0x710000888	14	1
280	140	L30-m0(4)	0x710000460	17-4	2	0	0	0x710000888	18	0
281	140	Dp1_l20(8)	0x710000460	17-4	2	1	0	0x710000888	18	1
282	141	L30-m0(5)	0x710000468	17-5	2	0	0	0x710000888	22	0
283	141	Dp1_l20(9)	0x710000468	17-5	2	1	0	0x710000888	22	1
284	142	L30-m0(6)	0x710000470	17-6	2	0	0	0x710000888	26	0
285	142	Dp1_l20(10)	0x710000470	17-6	2	1	0	0x710000888	26	1
286	143	L30-m0(7)	0x710000478	17-7	2	0	0	0x710000888	30	0
287	143	Dp1_l20(11)	0x710000478	17-7	2	1	0	0x710000888	30	1
288	144	L30-m0(8)	0x710000480	18-0	2	0	0	0x710000890	2	0
289	144	Dp1_l20(12)	0x710000480	18-0	2	1	0	0x710000890	2	1
290	145	L30-m0(9)	0x710000488	18-1	2	0	0	0x710000890	6	0
291	145	Dp1_l20(13)	0x710000488	18-1	2	1	0	0x710000890	6	1
292	146	L30-m0(10)	0x710000490	18-2	2	0	0	0x710000890	10	0
293	146	Dp1_l20(14)	0x710000490	18-2	2	1	0	0x710000890	10	1
294	147	L30-m0(11)	0x710000498	18-3	2	0	0	0x710000890	14	0
295	147	Dp1_l20(15)	0x710000498	18-3	2	1	0	0x710000890	14	1
296	148	L30-m0(12)	0x7100004a0	18-4	2	0	0	0x710000890	18	0
297	148	Dp1_l20(16)	0x7100004a0	18-4	2	1	0	0x710000890	18	1
298	149	L30-m0(13)	0x7100004a8	18-5	2	0	0	0x710000890	22	0

299	149	Dp1_l20(17)	0x7100004a8	18-5	2	1	0	0x710000890	22	1
300	150	L30-m0(14)	0x7100004b0	18-6	2	0	0	0x710000890	26	0
301	150	Dp1_l20(18)	0x7100004b0	18-6	2	1	0	0x710000890	26	1
302	151	L30-m0(15)	0x7100004b8	18-7	2	0	0	0x710000890	30	0
303	151	Dp1_l20(19)	0x7100004b8	18-7	2	1	0	0x710000890	30	1
304	152	L30-m0(16)	0x7100004c0	19-0	2	0	0	0x710000898	2	0
305	152	Dp1_l20(20)	0x7100004c0	19-0	2	1	0	0x710000898	2	1
306	153	L30-m0(17)	0x7100004c8	19-1	2	0	0	0x710000898	6	0
307	153	Dp1_l20(21)	0x7100004c8	19-1	2	1	0	0x710000898	6	1
308	154	L30-m0(18)	0x7100004d0	19-2	2	0	0	0x710000898	10	0
309	154	Dp1_l20(22)	0x7100004d0	19-2	2	1	0	0x710000898	10	1
310	155	L30-m0(19)	0x7100004d8	19-3	2	0	0	0x710000898	14	0
311	155	Dp1_l20(23)	0x7100004d8	19-3	2	1	0	0x710000898	14	1
312	156	L31-m0(0)	0x7100004e0	19-4	2	0	0	0x710000898	18	0
313	156	Dp1_l20(24)	0x7100004e0	19-4	2	1	0	0x710000898	18	1
314	157	L31-m0(1)	0x7100004e8	19-5	2	0	0	0x710000898	22	0
315	157	Dp1_l20(25)	0x7100004e8	19-5	2	1	0	0x710000898	22	1
316	158	L31-m0(2)	0x7100004f0	19-6	2	0	0	0x710000898	26	0
317	158	Dp1_l20(26)	0x7100004f0	19-6	2	1	0	0x710000898	26	1
318	159	L31-m0(3)	0x7100004f8	19-7	2	0	0	0x710000898	30	0
319	159	Dp1_l20(27)	0x7100004f8	19-7	2	1	0	0x710000898	30	1
320	160	L31-m0(4)	0x710000500	20-0	2	0	0	0x7100008a0	2	0
321	160	Dp1_l20(28)	0x710000500	20-0	2	1	0	0x7100008a0	2	1
322	161	L31-m0(5)	0x710000508	20-1	2	0	0	0x7100008a0	6	0
323	161	Dp1_l20(29)	0x710000508	20-1	2	1	0	0x7100008a0	6	1
324	162	L31-m0(6)	0x710000510	20-2	2	0	0	0x7100008a0	10	0
325	162	Dp1_l20(30)	0x710000510	20-2	2	1	0	0x7100008a0	10	1
326	163	L31-m0(7)	0x710000518	20-3	2	0	0	0x7100008a0	14	0
327	163	Dp1_l20(31)	0x710000518	20-3	2	1	0	0x7100008a0	14	1
328	164	L31-m0(8)	0x710000520	20-4	2	0	0	0x7100008a0	18	0
329	164	Dp1_l21(0)	0x710000520	20-4	2	1	0	0x7100008a0	18	1
330	165	L31-m0(9)	0x710000528	20-5	2	0	0	0x7100008a0	22	0
331	165	Dp1_l21(1)	0x710000528	20-5	2	1	0	0x7100008a0	22	1
332	166	L31-m0(10)	0x710000530	20-6	2	0	0	0x7100008a0	26	0
333	166	Dp1_l21(2)	0x710000530	20-6	2	1	0	0x7100008a0	26	1
334	167	L31-m0(11)	0x710000538	20-7	2	0	0	0x7100008a0	30	0
335	167	Dp1_l21(3)	0x710000538	20-7	2	1	0	0x7100008a0	30	1
336	168	L31-m0(12)	0x710000540	21-0	2	0	0	0x7100008a8	2	0
337	168	Dp1_l21(4)	0x710000540	21-0	2	1	0	0x7100008a8	2	1
338	169	L31-m0(13)	0x710000548	21-1	2	0	0	0x7100008a8	6	0
339	169	Dp1_l21(5)	0x710000548	21-1	2	1	0	0x7100008a8	6	1
340	170	L31-m0(14)	0x710000550	21-2	2	0	0	0x7100008a8	10	0
341	170	Dp1_l21(6)	0x710000550	21-2	2	1	0	0x7100008a8	10	1
342	171	L31-m0(15)	0x710000558	21-3	2	0	0	0x7100008a8	14	0
343	171	Dp1_l21(7)	0x710000558	21-3	2	1	0	0x7100008a8	14	1
344	172	L31-m0(16)	0x710000560	21-4	2	0	0	0x7100008a8	18	0
345	172	Dp1_l21(8)	0x710000560	21-4	2	1	0	0x7100008a8	18	1
346	173	L31-m0(17)	0x710000568	21-5	2	0	0	0x7100008a8	22	0
347	173	Dp1_l21(9)	0x710000568	21-5	2	1	0	0x7100008a8	22	1
348	174	L31-m0(18)	0x710000570	21-6	2	0	0	0x7100008a8	26	0
349	174	Dp1_l21(10)	0x710000570	21-6	2	1	0	0x7100008a8	26	1
350	175	L31-m0(19)	0x710000578	21-7	2	0	0	0x7100008a8	30	0
351	175	Dp1_l21(11)	0x710000578	21-7	2	1	0	0x7100008a8	30	1

352	176	Dp0_snp0(1)	0x710000580	22-0	2	0	0	0x7100008b0	2	0
353	176	Dp1_l21(12)	0x710000580	22-0	2	1	0	0x7100008b0	2	1
354	177	Dp0_snp0(2)	0x710000588	22-1	2	0	0	0x7100008b0	6	0
355	177	Dp1_l21(13)	0x710000588	22-1	2	1	0	0x7100008b0	6	1
356	178	Dp0_snp0(3)	0x710000590	22-2	2	0	0	0x7100008b0	10	0
357	178	Dp1_l21(14)	0x710000590	22-2	2	1	0	0x7100008b0	10	1
358	179	Dp0_snp0(4)	0x710000598	22-3	2	0	0	0x7100008b0	14	0
359	179	Dp1_l21(15)	0x710000598	22-3	2	1	0	0x7100008b0	14	1
360	180	Dp0_snp0(5)	0x7100005a0	22-4	2	0	0	0x7100008b0	18	0
361	180	Dp1_l21(16)	0x7100005a0	22-4	2	1	0	0x7100008b0	18	1
362	181	Dp0_snp0(6)	0x7100005a8	22-5	2	0	0	0x7100008b0	22	0
363	181	Dp1_l21(17)	0x7100005a8	22-5	2	1	0	0x7100008b0	22	1
364	182	Dp0_snp0(7)	0x7100005b0	22-6	2	0	0	0x7100008b0	26	0
365	182	Dp1_l21(18)	0x7100005b0	22-6	2	1	0	0x7100008b0	26	1
366	183	Dp0_snp0(8)	0x7100005b8	22-7	2	0	0	0x7100008b0	30	0
367	183	Dp1_l21(19)	0x7100005b8	22-7	2	1	0	0x7100008b0	30	1
368	184	Dp0_snp0(9)	0x7100005c0	23-0	2	0	0	0x7100008b8	2	0
369	184	Dp1_l21(20)	0x7100005c0	23-0	2	1	0	0x7100008b8	2	1
370	185	Dp0_snp1(1)	0x7100005c8	23-1	2	0	0	0x7100008b8	6	0
371	185	Dp1_l21(21)	0x7100005c8	23-1	2	1	0	0x7100008b8	6	1
372	186	Dp0_snp1(2)	0x7100005d0	23-2	2	0	0	0x7100008b8	10	0
373	186	Dp1_l21(22)	0x7100005d0	23-2	2	1	0	0x7100008b8	10	1
374	187	Dp0_snp1(3)	0x7100005d8	23-3	2	0	0	0x7100008b8	14	0
375	187	Dp1_l21(23)	0x7100005d8	23-3	2	1	0	0x7100008b8	14	1
376	188	Dp0_snp1(4)	0x7100005e0	23-4	2	0	0	0x7100008b8	18	0
377	188	Dp1_l21(24)	0x7100005e0	23-4	2	1	0	0x7100008b8	18	1
378	189	Dp0_snp1(5)	0x7100005e8	23-5	2	0	0	0x7100008b8	22	0
379	189	Dp1_l21(25)	0x7100005e8	23-5	2	1	0	0x7100008b8	22	1
380	190	Dp0_snp1(6)	0x7100005f0	23-6	2	0	0	0x7100008b8	26	0
381	190	Dp1_l21(26)	0x7100005f0	23-6	2	1	0	0x7100008b8	26	1
382	191	Dp0_snp1(7)	0x7100005f8	23-7	2	0	0	0x7100008b8	30	0
383	191	Dp1_l21(27)	0x7100005f8	23-7	2	1	0	0x7100008b8	30	1
384	192	Dp0_snp1(8)	0x710000600	24-0	2	0	0	0x7100008c0	2	0
385	192	Dp1_l21(28)	0x710000600	24-0	2	1	0	0x7100008c0	2	1
386	193	Dp0_snp1(9)	0x710000608	24-1	2	0	0	0x7100008c0	6	0
387	193	Dp1_l21(29)	0x710000608	24-1	2	1	0	0x7100008c0	6	1
388	194	Td_torus(0)	0x710000610	24-2	2	0	0	0x7100008c0	10	0
389	194	Dp1_l21(30)	0x710000610	24-2	2	1	0	0x7100008c0	10	1
390	195	Td_torus(1)	0x710000618	24-3	2	0	0	0x7100008c0	14	0
391	195	Dp1_l21(31)	0x710000618	24-3	2	1	0	0x7100008c0	14	1
392	196	Td_torus(2)	0x710000620	24-4	2	0	0	0x7100008c0	18	0
393	196	L30-m1(0)	0x710000620	24-4	2	1	0	0x7100008c0	18	1
394	197	Td_torus(3)	0x710000628	24-5	2	0	0	0x7100008c0	22	0
395	197	L30-m1(1)	0x710000628	24-5	2	1	0	0x7100008c0	22	1
396	198	Td_torus(4)	0x710000630	24-6	2	0	0	0x7100008c0	26	0
397	198	L30-m1(2)	0x710000630	24-6	2	1	0	0x7100008c0	26	1
398	199	Td_torus(5)	0x710000638	24-7	2	0	0	0x7100008c0	30	0
399	199	L30-m1(3)	0x710000638	24-7	2	1	0	0x7100008c0	30	1
400	200	Td_torus(6)	0x710000640	25-0	2	0	0	0x7100008c8	2	0
401	200	L30-m1(4)	0x710000640	25-0	2	1	0	0x7100008c8	2	1
402	201	Td_torus(7)	0x710000648	25-1	2	0	0	0x7100008c8	6	0
403	201	L30-m1(5)	0x710000648	25-1	2	1	0	0x7100008c8	6	1
404	202	Td_torus(8)	0x710000650	25-2	2	0	0	0x7100008c8	10	0

405	202	L30-m1(6)	0x710000650	25-2	2	1	0	0x7100008c8	10	1
406	203	Td_torus(9)	0x710000658	25-3	2	0	0	0x7100008c8	14	0
407	203	L30-m1(7)	0x710000658	25-3	2	1	0	0x7100008c8	14	1
408	204	Td_torus(10)	0x710000660	25-4	2	0	0	0x7100008c8	18	0
409	204	L30-m1(8)	0x710000660	25-4	2	1	0	0x7100008c8	18	1
410	205	Td_torus(11)	0x710000668	25-5	2	0	0	0x7100008c8	22	0
411	205	L30-m1(9)	0x710000668	25-5	2	1	0	0x7100008c8	22	1
412	206	Td_dma(0)	0x710000670	25-6	2	0	0	0x7100008c8	26	0
413	206	L30-m1(10)	0x710000670	25-6	2	1	0	0x7100008c8	26	1
414	207	Td_dma(1)	0x710000678	25-7	2	0	0	0x7100008c8	30	0
415	207	L30-m1(11)	0x710000678	25-7	2	1	0	0x7100008c8	30	1
416	208	Td_dma(2)	0x710000680	26-0	2	0	0	0x7100008d0	2	0
417	208	L30-m1(12)	0x710000680	26-0	2	1	0	0x7100008d0	2	1
418	209	Td_dma(3)	0x710000688	26-1	2	0	0	0x7100008d0	6	0
419	209	L30-m1(13)	0x710000688	26-1	2	1	0	0x7100008d0	6	1
420	210	Td_dma(4)	0x710000690	26-2	2	0	0	0x7100008d0	10	0
421	210	L30-m1(14)	0x710000690	26-2	2	1	0	0x7100008d0	10	1
422	211	Td_dma(5)	0x710000698	26-3	2	0	0	0x7100008d0	14	0
423	211	L30-m1(15)	0x710000698	26-3	2	1	0	0x7100008d0	14	1
424	212	Td_dma(6)	0x7100006a0	26-4	2	0	0	0x7100008d0	18	0
425	212	L30-m1(16)	0x7100006a0	26-4	2	1	0	0x7100008d0	18	1
426	213	Td_dma(7)	0x7100006a8	26-5	2	0	0	0x7100008d0	22	0
427	213	L30-m1(17)	0x7100006a8	26-5	2	1	0	0x7100008d0	22	1
428	214	Td_dma(8)	0x7100006b0	26-6	2	0	0	0x7100008d0	26	0
429	214	L30-m1(18)	0x7100006b0	26-6	2	1	0	0x7100008d0	26	1
430	215	Td_dma(9)	0x7100006b8	26-7	2	0	0	0x7100008d0	30	0
431	215	L30-m1(19)	0x7100006b8	26-7	2	1	0	0x7100008d0	30	1
432	216	Td_dma(10)	0x7100006c0	27-0	2	0	0	0x7100008d8	2	0
433	216	L31-m1(0)	0x7100006c0	27-0	2	1	0	0x7100008d8	2	1
434	217	Td_dma(11)	0x7100006c8	27-1	2	0	0	0x7100008d8	6	0
435	217	L31-m1(1)	0x7100006c8	27-1	2	1	0	0x7100008d8	6	1
436	218	Td_dma(12)	0x7100006d0	27-2	2	0	0	0x7100008d8	10	0
437	218	L31-m1(2)	0x7100006d0	27-2	2	1	0	0x7100008d8	10	1
438	219	Td_dma(13)	0x7100006d8	27-3	2	0	0	0x7100008d8	14	0
439	219	L31-m1(3)	0x7100006d8	27-3	2	1	0	0x7100008d8	14	1
440	220	Td_dma(14)	0x7100006e0	27-4	2	0	0	0x7100008d8	18	0
441	220	L31-m1(4)	0x7100006e0	27-4	2	1	0	0x7100008d8	18	1
442	221	Td_dma(15)	0x7100006e8	27-5	2	0	0	0x7100008d8	22	0
443	221	L31-m1(5)	0x7100006e8	27-5	2	1	0	0x7100008d8	22	1
444	222	Tr_m0(0)	0x7100006f0	27-6	2	0	0	0x7100008d8	26	0
445	222	L31-m1(6)	0x7100006f0	27-6	2	1	0	0x7100008d8	26	1
446	223	Tr_m0(1)	0x7100006f8	27-7	2	0	0	0x7100008d8	30	0
447	223	L31-m1(7)	0x7100006f8	27-7	2	1	0	0x7100008d8	30	1
448	224	Tr_m0(2)	0x710000700	28-0	2	0	0	0x7100008e0	2	0
449	224	L31-m1(8)	0x710000700	28-0	2	1	0	0x7100008e0	2	1
450	225	Tr_m0(3)	0x710000708	28-1	2	0	0	0x7100008e0	6	0
451	225	L31-m1(9)	0x710000708	28-1	2	1	0	0x7100008e0	6	1
452	226	Tr_m0(4)	0x710000710	28-2	2	0	0	0x7100008e0	10	0
453	226	L31-m1(10)	0x710000710	28-2	2	1	0	0x7100008e0	10	1
454	227	Tr_m0(5)	0x710000718	28-3	2	0	0	0x7100008e0	14	0
455	227	L31-m1(11)	0x710000718	28-3	2	1	0	0x7100008e0	14	1
456	228	Tr_m0(6)	0x710000720	28-4	2	0	0	0x7100008e0	18	0
457	228	L31-m1(12)	0x710000720	28-4	2	1	0	0x7100008e0	18	1

458	229	Tr_m0(7)	0x710000728	28-5	2	0	0	0x7100008e0	22	0
459	229	L31-m1(13)	0x710000728	28-5	2	1	0	0x7100008e0	22	1
460	230	Tr_m0(8)	0x710000730	28-6	2	0	0	0x7100008e0	26	0
461	230	L31-m1(14)	0x710000730	28-6	2	1	0	0x7100008e0	26	1
462	231	Tr_m0(9)	0x710000738	28-7	2	0	0	0x7100008e0	30	0
463	231	L31-m1(15)	0x710000738	28-7	2	1	0	0x7100008e0	30	1
464	232	Tr_m0(10)	0x710000740	29-0	2	0	0	0x7100008e8	2	0
465	232	L31-m1(16)	0x710000740	29-0	2	1	0	0x7100008e8	2	1
466	233	Tr_m0(11)	0x710000748	29-1	2	0	0	0x7100008e8	6	0
467	233	L31-m1(17)	0x710000748	29-1	2	1	0	0x7100008e8	6	1
468	234	Tr_m0(12)	0x710000750	29-2	2	0	0	0x7100008e8	10	0
469	234	L31-m1(18)	0x710000750	29-2	2	1	0	0x7100008e8	10	1
470	235	Tr_m0(13)	0x710000758	29-3	2	0	0	0x7100008e8	14	0
471	235	L31-m1(19)	0x710000758	29-3	2	1	0	0x7100008e8	14	1
472	236	Tr_m0(14)	0x710000760	29-4	2	0	0	0x7100008e8	18	0
473	236	Dp1_snp0(1)	0x710000760	29-4	2	1	0	0x7100008e8	18	1
474	237	Tr_m0(15)	0x710000768	29-5	2	0	0	0x7100008e8	22	0
475	237	Dp1_snp0(2)	0x710000768	29-5	2	1	0	0x7100008e8	22	1
476	238	Tr_m0(16)	0x710000770	29-6	2	0	0	0x7100008e8	26	0
477	238	Dp1_snp0(3)	0x710000770	29-6	2	1	0	0x7100008e8	26	1
478	239	Tr_m0(17)	0x710000778	29-7	2	0	0	0x7100008e8	30	0
479	239	Dp1_snp0(4)	0x710000778	29-7	2	1	0	0x7100008e8	30	1
480	240	Tr_m0(18)	0x710000780	30-0	2	0	0	0x7100008f0	2	0
481	240	Dp1_snp0(5)	0x710000780	30-0	2	1	0	0x7100008f0	2	1
482	241	Tr_m0(19)	0x710000788	30-1	2	0	0	0x7100008f0	6	0
483	241	Dp1_snp0(6)	0x710000788	30-1	2	1	0	0x7100008f0	6	1
484	242	Tr_m0(20)	0x710000790	30-2	2	0	0	0x7100008f0	10	0
485	242	Dp1_snp0(7)	0x710000790	30-2	2	1	0	0x7100008f0	10	1
486	243	Tr_m0(21)	0x710000798	30-3	2	0	0	0x7100008f0	14	0
487	243	Dp1_snp0(8)	0x710000798	30-3	2	1	0	0x7100008f0	14	1
488	244	Tr_m0(22)	0x7100007a0	30-4	2	0	0	0x7100008f0	18	0
489	244	Dp1_snp0(9)	0x7100007a0	30-4	2	1	0	0x7100008f0	18	1
490	245	Tr_m0(23)	0x7100007a8	30-5	2	0	0	0x7100008f0	22	0
491	245	Dp1_snp1(1)	0x7100007a8	30-5	2	1	0	0x7100008f0	22	1
492	246	Tr_m0(24)	0x7100007b0	30-6	2	0	0	0x7100008f0	26	0
493	246	Dp1_snp1(2)	0x7100007b0	30-6	2	1	0	0x7100008f0	26	1
494	247	Tr_m0(25)	0x7100007b8	30-7	2	0	0	0x7100008f0	30	0
495	247	Dp1_snp1(3)	0x7100007b8	30-7	2	1	0	0x7100008f0	30	1
496	248	Tr_m0(26)	0x7100007c0	31-0	2	0	0	0x7100008f8	2	0
497	248	Dp1_snp1(4)	0x7100007c0	31-0	2	1	0	0x7100008f8	2	1
498	249	Tr_m0(27)	0x7100007c8	31-1	2	0	0	0x7100008f8	6	0
499	249	Dp1_snp1(5)	0x7100007c8	31-1	2	1	0	0x7100008f8	6	1
500	250	Tr_m0(28)	0x7100007d0	31-2	2	0	0	0x7100008f8	10	0
501	250	Dp1_snp1(6)	0x7100007d0	31-2	2	1	0	0x7100008f8	10	1
502	251	Tr_m0(29)	0x7100007d8	31-3	2	0	0	0x7100008f8	14	0
503	251	Dp1_snp1(7)	0x7100007d8	31-3	2	1	0	0x7100008f8	14	1
504	252	Ic_timestamp	0x7100007e0	31-4	2	0	0	0x7100008f8	18	0
505	252	Dp1_snp1(8)	0x7100007e0	31-4	2	1	0	0x7100008f8	18	1
506	253		0x7100007e8	31-5	2	0	0	0x7100008f8	22	0
507	253	Dp1_snp1(9)	0x7100007e8	31-5	2	1	0	0x7100008f8	22	1
508	254		0x7100007f0	31-6	2	0	0	0x7100008f8	26	0
509	254		0x7100007f0	31-6	2	1	0	0x7100008f8	26	1
510	255		0x7100007f8	31-7	2	0	0	0x7100008f8	30	0

511	255		0x7100007f8	31-7	2	1	0	0x7100008f8	30	1
512	0	Dp0-pp0(0)	0x710000000	0-0	1	2	1	0x710000800	2	0
513	0	Dp1_pp0(0)	0x710000000	0-0	1	3	1	0x710000800	2	1
514	1	Dp0-pp0(1)	0x710000008	0-1	1	2	1	0x710000800	6	0
515	1	Dp1_pp0(1)	0x710000008	0-1	1	3	1	0x710000800	6	1
516	2	Dp0-pp0(2)	0x710000010	0-2	1	2	1	0x710000800	10	0
517	2	Dp1_pp0(2)	0x710000010	0-2	1	3	1	0x710000800	10	1
518	3	Dp0-pp0(3)	0x710000018	0-3	1	2	1	0x710000800	14	0
519	3	Dp1_pp0(3)	0x710000018	0-3	1	3	1	0x710000800	14	1
520	4	Dp0-pp0(4)	0x710000020	0-4	1	2	1	0x710000800	18	0
521	4	Dp1_pp0(4)	0x710000020	0-4	1	3	1	0x710000800	18	1
522	5	Dp0-pp0(5)	0x710000028	0-5	1	2	1	0x710000800	22	0
523	5	Dp1_pp0(5)	0x710000028	0-5	1	3	1	0x710000800	22	1
524	6	Dp0-pp0(6)	0x710000030	0-6	1	2	1	0x710000800	26	0
525	6	Dp1_pp0(6)	0x710000030	0-6	1	3	1	0x710000800	26	1
526	7	Dp0-pp0(7)	0x710000038	0-7	1	2	1	0x710000800	30	0
527	7	Dp1_pp0(7)	0x710000038	0-7	1	3	1	0x710000800	30	1
528	8	Dp0-pp0(8)	0x710000040	1-0	1	2	1	0x710000808	2	0
529	8	Dp1_pp0(8)	0x710000040	1-0	1	3	1	0x710000808	2	1
530	9	Dp0-pp0(9)	0x710000048	1-1	1	2	1	0x710000808	6	0
531	9	Dp1_pp0(9)	0x710000048	1-1	1	3	1	0x710000808	6	1
532	10	Dp0-pp0(10)	0x710000050	1-2	1	2	1	0x710000808	10	0
533	10	Dp1_pp0(10)	0x710000050	1-2	1	3	1	0x710000808	10	1
534	11	Dp0-pp0(11)	0x710000058	1-3	1	2	1	0x710000808	14	0
535	11	Dp1_pp0(11)	0x710000058	1-3	1	3	1	0x710000808	14	1
536	12	Dp0-pp0(12)	0x710000060	1-4	1	2	1	0x710000808	18	0
537	12	Dp1_pp0(12)	0x710000060	1-4	1	3	1	0x710000808	18	1
538	13	Dp0-pp0(13)	0x710000068	1-5	1	2	1	0x710000808	22	0
539	13	Dp1_pp0(13)	0x710000068	1-5	1	3	1	0x710000808	22	1
540	14	Dp0-pp0(14)	0x710000070	1-6	1	2	1	0x710000808	26	0
541	14	Dp1_pp0(14)	0x710000070	1-6	1	3	1	0x710000808	26	1
542	15	Dp0-pp0(15)	0x710000078	1-7	1	2	1	0x710000808	30	0
543	15	Dp1_pp0(15)	0x710000078	1-7	1	3	1	0x710000808	30	1
544	16	Dp0-pp0(16)	0x710000080	2-0	1	2	1	0x710000810	2	0
545	16	Dp1_pp0(16)	0x710000080	2-0	1	3	1	0x710000810	2	1
546	17	Dp0-pp0(17)	0x710000088	2-1	1	2	1	0x710000810	6	0
547	17	Dp1_pp0(17)	0x710000088	2-1	1	3	1	0x710000810	6	1
548	18	Dp0-pp0(18)	0x710000090	2-2	1	2	1	0x710000810	10	0
549	18	Dp1_pp0(18)	0x710000090	2-2	1	3	1	0x710000810	10	1
550	19	Dp0-pp0(19)	0x710000098	2-3	1	2	1	0x710000810	14	0
551	19	Dp1_pp0(19)	0x710000098	2-3	1	3	1	0x710000810	14	1
552	20	Dp0-pp0(20)	0x7100000a0	2-4	1	2	1	0x710000810	18	0
553	20	Dp1_pp0(20)	0x7100000a0	2-4	1	3	1	0x710000810	18	1
554	21	Dp0-pp0(21)	0x7100000a8	2-5	1	2	1	0x710000810	22	0
555	21	Dp1_pp0(21)	0x7100000a8	2-5	1	3	1	0x710000810	22	1
556	22	Dp0-pp0(22)	0x7100000b0	2-6	1	2	1	0x710000810	26	0
557	22	Dp1_pp0(22)	0x7100000b0	2-6	1	3	1	0x710000810	26	1
558	23	Dp0-pp0(23)	0x7100000b8	2-7	1	2	1	0x710000810	30	0
559	23	Dp1_pp0(23)	0x7100000b8	2-7	1	3	1	0x710000810	30	1
560	24	Dp0-pp0(24)	0x7100000c0	3-0	1	2	1	0x710000818	2	0
561	24	Dp1_pp0(24)	0x7100000c0	3-0	1	3	1	0x710000818	2	1
562	25	Dp0-pp0(25)	0x7100000c8	3-1	1	2	1	0x710000818	6	0
563	25	Dp1_pp0(25)	0x7100000c8	3-1	1	3	1	0x710000818	6	1

564	26	Dp0-pp0(26)	0x7100000d0	3-2	1	2	1	0x710000818	10	0
565	26	Dp1_pp0(26)	0x7100000d0	3-2	1	3	1	0x710000818	10	1
566	27	Dp0-pp0(27)	0x7100000d8	3-3	1	2	1	0x710000818	14	0
567	27	Dp1_pp0(27)	0x7100000d8	3-3	1	3	1	0x710000818	14	1
568	28	Dp0-pp0(28)	0x7100000e0	3-4	1	2	1	0x710000818	18	0
569	28	Dp1_pp0(28)	0x7100000e0	3-4	1	3	1	0x710000818	18	1
570	29	Dp0-pp0(29)	0x7100000e8	3-5	1	2	1	0x710000818	22	0
571	29	Dp1_pp0(29)	0x7100000e8	3-5	1	3	1	0x710000818	22	1
572	30	Dp0-pp0(30)	0x7100000f0	3-6	1	2	1	0x710000818	26	0
573	30	Dp1_pp0(30)	0x7100000f0	3-6	1	3	1	0x710000818	26	1
574	31	Dp0-pp0(31)	0x7100000f8	3-7	1	2	1	0x710000818	30	0
575	31	Dp1_pp0(31)	0x7100000f0	3-7	1	3	1	0x710000818	30	1
576	32	Dp0-pp0(32)	0x710000100	4-0	1	2	1	0x710000820	2	0
577	32	Dp1_pp0(32)	0x710000100	4-0	1	3	1	0x710000820	2	1
578	33	Dp0-pp0(33)	0x710000108	4-1	1	2	1	0x710000820	6	0
579	33	Dp1_pp0(33)	0x710000108	4-1	1	3	1	0x710000820	6	1
580	34	Dp0-pp0(34)	0x710000110	4-2	1	2	1	0x710000820	10	0
581	34	Dp1_pp0(34)	0x710000110	4-2	1	3	1	0x710000820	10	1
582	35	Dp0-pp1(0)	0x710000118	4-3	1	2	1	0x710000820	14	0
583	35	Dp1-pp1(0)	0x710000118	4-3	1	3	1	0x710000820	14	1
584	36	Dp0-pp1(1)	0x710000120	4-4	1	2	1	0x710000820	18	0
585	36	Dp1-pp1(1)	0x710000120	4-4	1	3	1	0x710000820	18	1
586	37	Dp0-pp1(2)	0x710000128	4-5	1	2	1	0x710000820	22	0
587	37	Dp1-pp1(2)	0x710000128	4-5	1	3	1	0x710000820	22	1
588	38	Dp0-pp1(3)	0x710000130	4-6	1	2	1	0x710000820	26	0
589	38	Dp1-pp1(3)	0x710000130	4-6	1	3	1	0x710000820	26	1
590	39	Dp0-pp1(4)	0x710000138	4-7	1	2	1	0x710000820	30	0
591	39	Dp1-pp1(4)	0x710000138	4-7	1	3	1	0x710000820	30	1
592	40	Dp0-pp1(5)	0x710000140	5-0	1	2	1	0x710000828	2	0
593	40	Dp1-pp1(5)	0x710000140	5-0	1	3	1	0x710000828	2	1
594	41	Dp0-pp1(6)	0x710000148	5-1	1	2	1	0x710000828	6	0
595	41	Dp1-pp1(6)	0x710000148	5-1	1	3	1	0x710000828	6	1
596	42	Dp0-pp1(7)	0x710000150	5-2	1	2	1	0x710000828	10	0
597	42	Dp1-pp1(7)	0x710000150	5-2	1	3	1	0x710000828	10	1
598	43	Dp0-pp1(8)	0x710000158	5-3	1	2	1	0x710000828	14	0
599	43	Dp1-pp1(8)	0x710000158	5-3	1	3	1	0x710000828	14	1
600	44	Dp0-pp1(9)	0x710000160	5-4	1	2	1	0x710000828	18	0
601	44	Dp1-pp1(9)	0x710000160	5-4	1	3	1	0x710000828	18	1
602	45	Dp0-pp1(10)	0x710000168	5-5	1	2	1	0x710000828	22	0
603	45	Dp1-pp1(10)	0x710000168	5-5	1	3	1	0x710000828	22	1
604	46	Dp0-pp1(11)	0x710000170	5-6	1	2	1	0x710000828	26	0
605	46	Dp1-pp1(11)	0x710000170	5-6	1	3	1	0x710000828	26	1
606	47	Dp0-pp1(12)	0x710000178	5-7	1	2	1	0x710000828	30	0
607	47	Dp1-pp1(12)	0x710000178	5-7	1	3	1	0x710000828	30	1
608	48	Dp0-pp1(13)	0x710000180	6-0	1	2	1	0x710000830	2	0
609	48	Dp1-pp1(13)	0x710000180	6-0	1	3	1	0x710000830	2	1
610	49	Dp0-pp1(14)	0x710000188	6-1	1	2	1	0x710000830	6	0
611	49	Dp1-pp1(14)	0x710000188	6-1	1	3	1	0x710000830	6	1
612	50	Dp0-pp1(15)	0x710000190	6-2	1	2	1	0x710000830	10	0
613	50	Dp1-pp1(15)	0x710000190	6-2	1	3	1	0x710000830	10	1
614	51	Dp0-pp1(16)	0x710000198	6-3	1	2	1	0x710000830	14	0
615	51	Dp1-pp1(16)	0x710000198	6-3	1	3	1	0x710000830	14	1
616	52	Dp0-pp1(17)	0x7100001a0	6-4	1	2	1	0x710000830	18	0

617	52	Dp1-pp1(17)	0x7100001a0	6-4	1	3	1	0x710000830	18	1
618	53	Dp0-pp1(18)	0x7100001a8	6-5	1	2	1	0x710000830	22	0
619	53	Dp1-pp1(18)	0x7100001a8	6-5	1	3	1	0x710000830	22	1
620	54	Dp0-pp1(19)	0x7100001b0	6-6	1	2	1	0x710000830	26	0
621	54	Dp1-pp1(19)	0x7100001b0	6-6	1	3	1	0x710000830	26	1
622	55	Dp0-pp1(20)	0x7100001b8	6-7	1	2	1	0x710000830	30	0
623	55	Dp1-pp1(20)	0x7100001b8	6-7	1	3	1	0x710000830	30	1
624	56	Dp0-pp1(21)	0x7100001c0	7-0	1	2	1	0x710000838	2	0
625	56	Dp1-pp1(21)	0x7100001c0	7-0	1	3	1	0x710000838	2	1
626	57	Dp0-pp1(22)	0x7100001c8	7-1	1	2	1	0x710000838	6	0
627	57	Dp1-pp1(22)	0x7100001c8	7-1	1	3	1	0x710000838	6	1
628	58	Dp0-pp1(23)	0x7100001d0	7-2	1	2	1	0x710000838	10	0
629	58	Dp1-pp1(23)	0x7100001d0	7-2	1	3	1	0x710000838	10	1
630	59	Dp0-pp1(24)	0x7100001d8	7-3	1	2	1	0x710000838	14	0
631	59	Dp1-pp1(24)	0x7100001d8	7-3	1	3	1	0x710000838	14	1
632	60	Dp0-pp1(25)	0x7100001e0	7-4	1	2	1	0x710000838	18	0
633	60	Dp1-pp1(25)	0x7100001e0	7-4	1	3	1	0x710000838	18	1
634	61	Dp0-pp1(26)	0x7100001e8	7-5	1	2	1	0x710000838	22	0
635	61	Dp1-pp1(26)	0x7100001e8	7-5	1	3	1	0x710000838	22	1
636	62	Dp0-pp1(27)	0x7100001f0	7-6	1	2	1	0x710000838	26	0
637	62	Dp1-pp1(27)	0x7100001f0	7-6	1	3	1	0x710000838	26	1
638	63	Dp0-pp1(28)	0x7100001f8	7-7	1	2	1	0x710000838	30	0
639	63	Dp1-pp1(28)	0x7100001f8	7-7	1	3	1	0x710000838	30	1
640	64	Dp0-pp1(29)	0x710000200	8-0	1	2	1	0x710000840	2	0
641	64	Dp1-pp1(29)	0x710000200	8-0	1	3	1	0x710000840	2	1
642	65	Dp0-pp1(30)	0x710000208	8-1	1	2	1	0x710000840	6	0
643	65	Dp1-pp1(30)	0x710000208	8-1	1	3	1	0x710000840	6	1
644	66	Dp0-pp1(31)	0x710000210	8-2	1	2	1	0x710000840	10	0
645	66	Dp1-pp1(31)	0x710000210	8-2	1	3	1	0x710000840	10	1
646	67	Dp0-pp1(32)	0x710000218	8-3	1	2	1	0x710000840	14	0
647	67	Dp1-pp1(32)	0x710000218	8-3	1	3	1	0x710000840	14	1
648	68	Dp0-pp1(33)	0x710000220	8-4	1	2	1	0x710000840	18	0
649	68	Dp1-pp1(33)	0x710000220	8-4	1	3	1	0x710000840	18	1
650	69	Dp0-pp1(34)	0x710000228	8-5	1	2	1	0x710000840	22	0
651	69	Dp1-pp1(34)	0x710000228	8-5	1	3	1	0x710000840	22	1
652	70	Dp0-snp0(0)	0x710000230	8-6	1	2	1	0x710000840	26	0
653	70	Dp1-snp0(0)	0x710000230	8-6	1	3	1	0x710000840	26	1
654	71	Dp0-snp1(0)	0x710000238	8-7	1	2	1	0x710000840	30	0
655	71	Dp1-snp1(0)	0x710000238	8-7	1	3	1	0x710000840	30	1
656	72	Dp0-snp0(10)	0x710000240	9-0	2	2	1	0x710000848	2	0
657	72	Tr_m3(0)	0x710000240	9-0	2	3	1	0x710000848	2	1
658	73	Dp0-snp0(11)	0x710000248	9-1	2	2	1	0x710000848	6	0
659	73	Tr_m3(1)	0x710000248	9-1	2	3	1	0x710000848	6	1
660	74	Dp0-snp0(12)	0x710000250	9-2	2	2	1	0x710000848	10	0
661	74	Tr_m3(2)	0x710000250	9-2	2	3	1	0x710000848	10	1
662	75	Dp0-snp0(13)	0x710000258	9-3	2	2	1	0x710000848	14	0
663	75	Tr_m3(3)	0x710000258	9-3	2	3	1	0x710000848	14	1
664	76	Dp0-snp0(14)	0x710000260	9-4	2	2	1	0x710000848	18	0
665	76	Tr_m3(4)	0x710000260	9-4	2	3	1	0x710000848	18	1
666	77	Dp0-snp0(15)	0x710000266	9-5	2	2	1	0x710000848	22	0
667	77	Tr_m3(5)	0x710000266	9-5	2	3	1	0x710000848	22	1
668	78	Dp0-snp0(16)	0x710000270	9-6	2	2	1	0x710000848	26	0
669	78	Tr_m3(6)	0x710000270	9-6	2	3	1	0x710000848	26	1

670	79	Dp0-snp0(17)	0x710000278	9-7	2	2	1	0x710000848	30	0
671	79	Tr_m3(7)	0x710000278	9-7	2	3	1	0x710000848	30	1
672	80	Dp0-snp0(18)	0x710000280	10-0	2	2	1	0x710000850	2	0
673	80	Tr_m3(8)	0x710000280	10-0	2	3	1	0x710000850	2	1
674	81	Dp0-snp0(19)	0x710000288	10-1	2	2	1	0x710000850	6	0
675	81	Tr_m3(9)	0x710000288	10-1	2	3	1	0x710000850	6	1
676	82	Dp0-snp0(20)	0x710000290	10-2	2	2	1	0x710000850	10	0
677	82	Tr_m3(10)	0x710000290	10-2	2	3	1	0x710000850	10	1
678	83	Dp0-snp0(21)	0x710000298	10-3	2	2	1	0x710000850	14	0
679	83	Tr_m3(11)	0x710000298	10-3	2	3	1	0x710000850	14	1
680	84	Dp0-snp0(22)	0x7100002a0	10-4	2	2	1	0x710000850	18	0
681	84	Tr_m3(12)	0x7100002a0	10-4	2	3	1	0x710000850	18	1
682	85	Dp0-snp0(23)	0x7100002a8	10-5	2	2	1	0x710000850	22	0
683	85	Tr_m3(13)	0x7100002a8	10-5	2	3	1	0x710000850	22	1
684	86	Dp0-snp0(24)	0x7100002b0	10-6	2	2	1	0x710000850	26	0
685	86	Tr_m3(14)	0x7100002b0	10-6	2	3	1	0x710000850	26	1
686	87	Dp0-snp0(25)	0x7100002b8	10-7	2	2	1	0x710000850	30	0
687	87	Tr_m3(15)	0x7100002b8	10-7	2	3	1	0x710000850	30	1
688	88	Dp0-snp0(26)	0x7100002c0	11-0	2	2	1	0x710000858	2	0
689	88	Tr_m3(16)	0x7100002c0	11-0	2	3	1	0x710000858	2	1
690	89	Dp0-snp0(27)	0x7100002c8	11-1	2	2	1	0x710000858	6	0
691	89	Tr_m3(17)	0x7100002c8	11-1	2	3	1	0x710000858	6	1
692	90	Dp0-snp0(28)	0x7100002d0	11-2	2	2	1	0x710000858	10	0
693	90	Tr_m3(18)	0x7100002d0	11-2	2	3	1	0x710000858	10	1
694	91	Dp0-snp0(29)	0x7100002d8	11-3	2	2	1	0x710000858	14	0
695	91	Tr_m3(19)	0x7100002d8	11-3	2	3	1	0x710000858	14	1
696	92	Dp0-snp0(30)	T0x7100002e0	11-4	2	2	1	0x710000858	18	0
697	92	Tr_m3(20)	0x7100002e0	11-4	2	3	1	0x710000858	18	1
698	93	Dp0-snp0(31)	0x7100002e8	11-5	2	2	1	0x710000858	22	0
699	93	Tr_m3(21)	0x7100002e8	11-5	2	3	1	0x710000858	22	1
700	94	Dp0-snp0(32)	0x7100002f0	11-6	2	2	1	0x710000858	26	0
701	94	Tr_m3(22)	0x7100002f0	11-6	2	3	1	0x710000858	26	1
702	95	Dp0-snp0(33)	0x7100002f8	11-7	2	2	1	0x710000858	30	0
703	95	Tr_m3(23)	0x7100002f8	11-7	2	3	1	0x710000858	30	1
704	96	Dp0-snp0(34)	0x710000300	12-0	2	2	1	0x710000860	2	0
705	96	Tr_m3(24)	0x710000300	12-0	2	3	1	0x710000860	2	1
706	97	Dp0-snp0(35)	0x710000308	12-1	2	2	1	0x710000860	6	0
707	97	Tr_m3(25)	0x710000308	12-1	2	3	1	0x710000860	6	1
708	98	Dp0-snp0(36)	0x710000310	12-2	2	2	1	0x710000860	10	0
709	98	Tr_m3(26)	0x710000310	12-2	2	3	1	0x710000860	10	1
710	99	Dp0-snp0(37)	0x710000318	12-3	2	2	1	0x710000860	14	0
711	99	Tr_m3(27)	0x710000318	12-3	2	3	1	0x710000860	14	1
712	100	Dp0-snp1(10)	0x710000320	12-4	2	2	1	0x710000860	18	0
713	100	Tr_m3(28)	0x710000320	12-4	2	3	1	0x710000860	18	1
714	101	Dp0-snp1(11)	0x710000328	12-5	2	2	1	0x710000860	22	0
715	101	Tr_m3(29)	0x710000328	12-5	2	3	1	0x710000860	22	1
716	102	Dp0-snp1(12)	0x710000330	12-6	2	2	1	0x710000860	26	0
717	102	Tr_m3(30)	0x710000330	12-6	2	3	1	0x710000860	26	1
718	103	Dp0-snp1(13)	0x710000338	12-7	2	2	1	0x710000860	30	0
719	103	Tr_m3(31)	0x710000338	12-7	2	3	1	0x710000860	30	1
720	104	Dp0-snp1(14)	0x710000340	13-0	2	2	1	0x710000868	2	0
721	104	Tr_m3(32)	0x710000340	13-0	2	3	1	0x710000868	2	1
722	105	Dp0-snp1(15)	0x710000348	13-1	2	2	1	0x710000868	6	0

723	105	Tr_m3(33)	0x710000348	13-1	2	3	1	0x710000868	6	1
724	106	Dp0-snp1(16)	0x710000350	13-2	2	2	1	0x710000868	10	0
725	106	Tr_m3(34)	0x710000350	13-2	2	3	1	0x710000868	10	1
726	107	Dp0-snp1(17)	0x710000358	13-3	2	2	1	0x710000868	14	0
727	107	Tr_m3(35)	0x710000358	13-3	2	3	1	0x710000868	14	1
728	108	Dp0-snp1(18)	0x710000360	13-4	2	2	1	0x710000868	18	0
729	108	Tr_m3(36)	0x710000360	13-4	2	3	1	0x710000868	18	1
730	109	Dp0-snp1(19)	0x710000368	13-5	2	2	1	0x710000868	22	0
731	109	Tr_m3(37)	0x710000368	13-5	2	3	1	0x710000868	22	1
732	110	Dp0-snp1(20)	0x710000370	13-6	2	2	1	0x710000868	26	0
733	110	Tr_m3(38)	0x710000370	13-6	2	3	1	0x710000868	26	1
734	111	Dp0-snp1(21)	0x710000378	13-7	2	2	1	0x710000868	30	0
735	111	Tr_m3(39)	0x710000378	13-7	2	3	1	0x710000868	30	1
736	112	Dp0-snp1(22)	0x710000380	14-0	2	2	1	0x710000870	2	0
737	112	Tr_m3(40)	0x710000380	14-0	2	3	1	0x710000870	2	1
738	113	Dp0-snp1(23)	0x710000388	14-1	2	2	1	0x710000870	6	0
739	113	Tr_m3(41)	0x710000388	14-1	2	3	1	0x710000870	6	1
740	114	Dp0-snp1(24)	0x710000390	14-2	2	2	1	0x710000870	10	0
741	114	Tr_m3(42)	0x710000390	14-2	2	3	1	0x710000870	10	1
742	115	Dp0-snp1(25)	0x710000398	14-3	2	2	1	0x710000870	14	0
743	115	Tr_m3(43)	0x710000398	14-3	2	3	1	0x710000870	14	1
744	116	Dp0-snp1(26)	0x7100003a0	14-4	2	2	1	0x710000870	18	0
745	116	Tr_m3(44)	0x7100003a0	14-4	2	3	1	0x710000870	18	1
746	117	Dp0-snp1(27)	0x7100003a8	14-5	2	2	1	0x710000870	22	0
747	117	Tr_m3(45)	0x7100003a8	14-5	2	3	1	0x710000870	22	1
748	118	Dp0-snp1(28)	0x7100003b0	14-6	2	2	1	0x710000870	26	0
749	118	Tr_m3(46)	0x7100003b0	14-6	2	3	1	0x710000870	26	1
750	119	Dp0-snp1(29)	0x7100003b8	14-7	2	2	1	0x710000870	30	0
751	119	Tr_m3(47)	0x7100003b8	14-7	2	3	1	0x710000870	30	1
752	120	Dp0-snp1(30)	0x7100003c0	15-0	2	2	1	0x710000878	2	0
753	120	Tr_m3(48)	0x7100003c0	15-0	2	3	1	0x710000878	2	1
754	121	Dp0-snp1(31)	0x7100003c8	15-1	2	2	1	0x710000878	6	0
755	121	Tr_m3(49)	0x7100003c8	15-1	2	3	1	0x710000878	6	1
756	122	Dp0-snp1(32)	0x7100003d0	15-2	2	2	1	0x710000878	10	0
757	122	Tr_m3(50)	0x7100003d0	15-2	2	3	1	0x710000878	10	1
758	123	Dp0-snp1(33)	0x7100003d8	15-3	2	2	1	0x710000878	14	0
759	123	Tr_m3(51)	0x7100003d8	15-3	2	3	1	0x710000878	14	1
760	124	Dp0-snp1(34)	0x7100003e0	15-4	2	2	1	0x710000878	18	0
761	124	Tr_m3(52)	0x7100003e0	15-4	2	3	1	0x710000878	18	1
762	125	Dp0-snp1(35)	0x7100003e8	15-5	2	2	1	0x710000878	22	0
763	125	Tr_m3(53)	0x7100003e8	15-5	2	3	1	0x710000878	22	1
764	126	Dp0-snp1(36)	0x7100003f0	15-6	2	2	1	0x710000878	26	0
765	126	Tr_m3(54)	0x7100003f0	15-6	2	3	1	0x710000878	26	1
766	127	Dp0-snp1(37)	0x7100003f8	15-7	2	2	1	0x710000878	30	0
767	127	Tr_m3(55)	0x7100003f8	15-7	2	3	1	0x710000878	30	1
768	128	Td_torus(12)	0x710000400	16-0	2	2	1	0x710000880	2	0
769	128	Tr_m3(56)	0x710000400	16-0	2	3	1	0x710000880	2	1
770	129	Td_torus(13)	0x710000408	16-1	2	2	1	0x710000880	6	0
771	129	Tr_m3(57)	0x710000408	16-1	2	3	1	0x710000880	6	1
772	130	Td_torus(14)	0x710000410	16-2	2	2	1	0x710000880	10	0
773	130	Tr_m3(58)	0x710000410	16-2	2	3	1	0x710000880	10	1
774	131	Td_torus(15)	0x710000418	16-3	2	2	1	0x710000880	14	0
775	131	Tr_m3(59)	0x710000418	16-3	2	3	1	0x710000880	14	1

776	132	Td_torus(16)	0x710000420	16-4	2	2	1	0x710000880	18	0
777	132	Tr_m3(60)	0x710000420	16-4	2	3	1	0x710000880	18	1
778	133	Td_torus(17)	0x710000428	16-5	2	2	1	0x710000880	22	0
779	133	Tr_m3(61)	0x710000428	16-5	2	3	1	0x710000880	22	1
780	134	Td_torus(18)	0x710000430	16-6	2	2	1	0x710000880	26	0
781	134	Tr_m3(62)	0x710000430	16-6	2	3	1	0x710000880	26	1
782	135	Td_torus(19)	0x710000438	16-7	2	2	1	0x710000880	30	0
783	135	Tr_m3(63)	0x710000438	16-7	2	3	1	0x710000880	30	1
784	136	Td_torus(20)	0x710000440	17-0	2	2	1	0x710000888	2	0
785	136	Tr_m3(64)	0x710000440	17-0	2	3	1	0x710000888	2	1
786	137	Td_torus(21)	0x710000448	17-1	2	2	1	0x710000888	6	0
787	137	Tr_m3(65)	0x710000448	17-1	2	3	1	0x710000888	6	1
788	138	Td_torus(22)	0x710000450	17-2	2	2	1	0x710000888	10	0
789	138	Tr_m3(66)	0x710000450	17-2	2	3	1	0x710000888	10	1
790	139	Td_torus(23)	0x710000458	17-3	2	2	1	0x710000888	14	0
791	139	Tr_m3(67)	0x710000458	17-3	2	3	1	0x710000888	14	1
792	140	Td_torus(24)	0x710000460	17-4	2	2	1	0x710000888	18	0
793	140	Tr_m3(68)	0x710000460	17-4	2	3	1	0x710000888	18	1
794	141	Td_torus(25)	0x710000468	17-5	2	2	1	0x710000888	22	0
795	141	Tr_m3(69)	0x710000468	17-5	2	3	1	0x710000888	22	1
796	142	Td_torus(26)	0x710000470	17-6	2	2	1	0x710000888	26	0
797	142	Tr_m3(70)	0x710000470	17-6	2	3	1	0x710000888	26	1
798	143	Td_torus(27)	0x710000478	17-7	2	2	1	0x710000888	30	0
799	143	Tr_m3(71)	0x710000478	17-7	2	3	1	0x710000888	30	1
800	144	Td_torus(28)	0x710000480	18-0	2	2	1	0x710000890	2	0
801	144	Tr_m3(72)	0x710000480	18-0	2	3	1	0x710000890	2	1
802	145	Td_torus(29)	0x710000488	18-1	2	2	1	0x710000890	6	0
803	145	Tr_m3(73)	0x710000488	18-1	2	3	1	0x710000890	6	1
804	146	Td_torus(30)	0x710000490	18-2	2	2	1	0x710000890	10	0
805	146	Tr_m3(74)	0x710000490	18-2	2	3	1	0x710000890	10	1
806	147	Td_torus(31)	0x710000498	18-3	2	2	1	0x710000890	14	0
807	147	Dp1_snp0(10)	0x710000498	18-3	2	3	1	0x710000890	14	1
808	148	Td_torus(32)	0x7100004a0	18-4	2	2	1	0x710000890	18	0
809	148	Dp1_snp0(11)	0x7100004a0	18-4	2	3	1	0x710000890	18	1
810	149	Td_torus(33)	0x7100004a8	18-5	2	2	1	0x710000890	22	0
811	149	Dp1_snp0(12)	0x7100004a8	18-5	2	3	1	0x710000890	22	1
812	150	Td_torus(34)	0x7100004b0	18-6	2	2	1	0x710000890	26	0
813	150	Dp1_snp0(13)	0x7100004b0	18-6	2	3	1	0x710000890	26	1
814	151	Td_torus(35)	0x7100004b8	18-7	2	2	1	0x710000890	30	0
815	151	Dp1_snp0(14)	0x7100004b8	18-7	2	3	1	0x710000890	30	1
816	152	Td_torus(36)	0x7100004c0	19-0	2	2	1	0x710000898	2	0
817	152	Dp1_snp0(15)	0x7100004c0	19-0	2	3	1	0x710000898	2	1
818	153	Td_torus(37)	0x7100004c8	19-1	2	2	1	0x710000898	6	0
819	153	Dp1_snp0(16)	0x7100004c8	19-1	2	3	1	0x710000898	6	1
820	154	Td_torus(38)	0x7100004d0	19-2	2	2	1	0x710000898	10	0
821	154	Dp1_snp0(17)	0x7100004d0	19-2	2	3	1	0x710000898	10	1
822	155	Td_torus(39)	0x7100004d8	19-3	2	2	1	0x710000898	14	0
823	155	Dp1_snp0(18)	0x7100004d8	19-3	2	3	1	0x710000898	14	1
824	156	Td_torus(40)	0x7100004e0	19-4	2	2	1	0x710000898	18	0
825	156	Dp1_snp0(19)	0x7100004e0	19-4	2	3	1	0x710000898	18	1
826	157	Td_torus(41)	0x7100004e8	19-5	2	2	1	0x710000898	22	0
827	157	Dp1_snp0(20)	0x7100004e8	19-5	2	3	1	0x710000898	22	1
828	158	Td_torus(42)	0x7100004f0	19-6	2	2	1	0x710000898	26	0

829	158	Dp1_snp0(21)	0x7100004f0	19-6	2	3	1	0x710000898	26	1
830	159	Td_torus(43)	0x7100004f8	19-7	2	2	1	0x710000898	30	0
831	159	Dp1_snp0(22)	0x7100004f8	19-7	2	3	1	0x710000898	30	1
832	160	Td_torus(44)	0x710000500	20-0	2	2	1	0x7100008a0	2	0
833	160	Dp1_snp0(23)	0x710000500	20-0	2	3	1	0x7100008a0	2	1
834	161	Td_torus(45)	0x710000508	20-1	2	2	1	0x7100008a0	6	0
835	161	Dp1_snp0(24)	0x710000508	20-1	2	3	1	0x7100008a0	6	1
836	162	Td_torus(46)	0x710000510	20-2	2	2	1	0x7100008a0	10	0
837	162	Dp1_snp0(25)	0x710000510	20-2	2	3	1	0x7100008a0	10	1
838	163	Td_torus(47)	0x710000518	20-3	2	2	1	0x7100008a0	14	0
839	163	Dp1_snp0(26)	0x710000518	20-3	2	3	1	0x7100008a0	14	1
840	164	Td_torus(48)	0x710000520	20-4	2	2	1	0x7100008a0	18	0
841	164	Dp1_snp0(27)	0x710000520	20-4	2	3	1	0x7100008a0	18	1
842	165	Td_torus(49)	0x710000528	20-5	2	2	1	0x7100008a0	22	0
843	165	Dp1_snp0(28)	0x710000528	20-5	2	3	1	0x7100008a0	22	1
844	166	Td_torus(50)	0x710000530	20-6	2	2	1	0x7100008a0	26	0
845	166	Dp1_snp0(29)	0x710000530	20-6	2	3	1	0x7100008a0	26	1
846	167	Td_torus(51)	0x710000538	20-7	2	2	1	0x7100008a0	30	0
847	167	Dp1_snp0(30)	0x710000538	20-7	2	3	1	0x7100008a0	30	1
848	168	Td_torus(52)	0x710000540	21-0	2	2	1	0x7100008a8	2	0
849	168	Dp1_snp0(31)	0x710000540	21-0	2	3	1	0x7100008a8	2	1
850	169	Td_torus(53)	0x710000548	21-1	2	2	1	0x7100008a8	6	0
851	169	Dp1_snp0(32)	0x710000548	21-1	2	3	1	0x7100008a8	6	1
852	170	Td_torus(54)	0x710000550	21-2	2	2	1	0x7100008a8	10	0
853	170	Dp1_snp0(33)	0x710000550	21-2	2	3	1	0x7100008a8	10	1
854	171	Td_torus(55)	0x710000558	21-3	2	2	1	0x7100008a8	14	0
855	171	Dp1_snp0(34)	0x710000558	21-3	2	3	1	0x7100008a8	14	1
856	172	Td_torus(56)	0x710000560	21-4	2	2	1	0x7100008a8	18	0
857	172	Dp1_snp0(35)	0x710000560	21-4	2	3	1	0x7100008a8	18	1
858	173	Td_torus(57)	0x710000568	21-5	2	2	1	0x7100008a8	22	0
859	173	Dp1_snp0(36)	0x710000568	21-5	2	3	1	0x7100008a8	22	1
860	174	Td_torus(58)	0x710000570	21-6	2	2	1	0x7100008a8	26	0
861	174	Dp1_snp0(37)	0x710000570	21-6	2	3	1	0x7100008a8	26	1
862	175	Td_torus(59)	0x710000578	21-7	2	2	1	0x7100008a8	30	0
863	175	Dp1_snp1(10)	0x710000578	21-7	2	3	1	0x7100008a8	30	1
864	176	Td_torus(60)	0x710000580	22-0	2	2	1	0x7100008b0	2	0
865	176	Dp1_snp1(11)	0x710000580	22-0	2	3	1	0x7100008b0	2	1
866	177	Td_torus(61)	0x710000588	22-1	2	2	1	0x7100008b0	6	0
867	177	Dp1_snp1(12)	0x710000588	22-1	2	3	1	0x7100008b0	6	1
868	178	Td_torus(62)	0x710000590	22-2	2	2	1	0x7100008b0	10	0
869	178	Dp1_snp1(13)	0x710000590	22-2	2	3	1	0x7100008b0	10	1
870	179	Td_torus(63)	0x710000598	22-3	2	2	1	0x7100008b0	14	0
871	179	Dp1_snp1(14)	0x710000598	22-3	2	3	1	0x7100008b0	14	1
872	180	Td_torus(64)	0x7100005a0	22-4	2	2	1	0x7100008b0	18	0
873	180	Dp1_snp1(15)	0x7100005a0	22-4	2	3	1	0x7100008b0	18	1
874	181	Td_torus(65)	0x7100005a8	22-5	2	2	1	0x7100008b0	22	0
875	181	Dp1_snp1(16)	0x7100005a8	22-5	2	3	1	0x7100008b0	22	1
876	182	Td_torus(66)	0x7100005b0	22-6	2	2	1	0x7100008b0	26	0
877	182	Dp1_snp1(17)	0x7100005b0	22-6	2	3	1	0x7100008b0	26	1
878	183	Td_torus(67)	0x7100005b8	22-7	2	2	1	0x7100008b0	30	0
879	183	Dp1_snp1(18)	0x7100005b8	22-7	2	3	1	0x7100008b0	30	1
880	184	Td_torus(68)	0x7100005c0	23-0	2	2	1	0x7100008b8	2	0
881	184	Dp1_snp1(19)	0x7100005c0	23-0	2	3	1	0x7100008b8	2	1

882	185	Td_torus(69)	0x7100005c8	23-1	2	2	1	0x7100008b8	6	0
883	185	Dp1_snp1(20)	0x7100005c8	23-1	2	3	1	0x7100008b8	6	1
884	186	Td_torus(70)	0x7100005d0	23-2	2	2	1	0x7100008b8	10	0
885	186	Dp1_snp1(21)	0x7100005d0	23-2	2	3	1	0x7100008b8	10	1
886	187	Td_torus(71)	0x7100005d8	23-3	2	2	1	0x7100008b8	14	0
887	187	Dp1_snp1(22)	0x7100005d8	23-3	2	3	1	0x7100008b8	14	1
888	188	Td_dma(16)	0x7100005e0	23-4	2	2	1	0x7100008b8	18	0
889	188	Dp1_snp1(23)	0x7100005e0	23-4	2	3	1	0x7100008b8	18	1
890	189	Td_dma(17)	0x7100005e8	23-5	2	2	1	0x7100008b8	22	0
891	189	Dp1_snp1(24)	0x7100005e8	23-5	2	3	1	0x7100008b8	22	1
892	190	Td_dma(18)	0x7100005f0	23-6	2	2	1	0x7100008b8	26	0
893	190	Dp1_snp1(25)	0x7100005f0	23-6	2	3	1	0x7100008b8	26	1
894	191	Td_dma(19)	0x7100005f8	23-7	2	2	1	0x7100008b8	30	0
895	191	Dp1_snp1(26)	0x7100005f8	23-7	2	3	1	0x7100008b8	30	1
896	192	Td_dma(20)	0x710000600	24-0	2	2	1	0x7100008c0	2	0
897	192	Dp1_snp1(27)	0x710000600	24-0	2	3	1	0x7100008c0	2	1
898	193	Td_dma(21)	0x710000608	24-1	2	2	1	0x7100008c0	6	0
899	193	Dp1_snp1(28)	0x710000608	24-1	2	3	1	0x7100008c0	6	1
900	194	Td_dma(22)	0x710000610	24-2	2	2	1	0x7100008c0	10	0
901	194	Dp1_snp1(29)	0x710000610	24-2	2	3	1	0x7100008c0	10	1
902	195	Td_dma(23)	0x710000618	24-3	2	2	1	0x7100008c0	14	0
903	195	Dp1_snp1(30)	0x710000618	24-3	2	3	1	0x7100008c0	14	1
904	196	Td_dma(24)	0x710000620	24-4	2	2	1	0x7100008c0	18	0
905	196	Dp1_snp1(31)	0x710000620	24-4	2	3	1	0x7100008c0	18	1
906	197	Td_dma(25)	0x710000628	24-5	2	2	1	0x7100008c0	22	0
907	197	Dp1_snp1(32)	0x710000628	24-5	2	3	1	0x7100008c0	22	1
908	198	Td_dma(26)	0x710000630	24-6	2	2	1	0x7100008c0	26	0
909	198	Dp1_snp1(33)	0x710000630	24-6	2	3	1	0x7100008c0	26	1
910	199	Td_dma(27)	0x710000638	24-7	2	2	1	0x7100008c0	30	0
911	199	Dp1_snp1(34)	0x710000638	24-7	2	3	1	0x7100008c0	30	1
912	200	Td_dma(28)	0x710000640	25-0	2	2	1	0x7100008c8	2	0
913	200	Dp1_snp1(35)	0x710000640	25-0	2	3	1	0x7100008c8	2	1
914	201	Td_dma(29)	0x710000648	25-1	2	2	1	0x7100008c8	6	0
915	201	Dp1_snp1(36)	0x710000648	25-1	2	3	1	0x7100008c8	6	1
916	202	Td_dma(30)	0x710000650	25-2	2	2	1	0x7100008c8	10	0
917	202	Dp1_snp1(37)	0x710000650	25-2	2	3	1	0x7100008c8	10	1
918	203	Td_dma(31)	0x710000658	25-3	2	2	1	0x7100008c8	14	0
919	203		0x710000658	25-3	2	3	1	0x7100008c8	14	1
920	204	Tr_m2(0)	0x710000660	25-4	2	2	1	0x7100008c8	18	0
921	204		0x710000660	25-4	2	3	1	0x7100008c8	18	1
922	205	Tr_m2(1)	0x710000668	25-5	2	2	1	0x7100008c8	22	0
923	205		0x710000668	25-5	2	3	1	0x7100008c8	22	1
924	206	Tr_m2(2)	0x710000670	25-6	2	2	1	0x7100008c8	26	0
925	206		0x710000670	25-6	2	3	1	0x7100008c8	26	1
926	207	Tr_m2(3)	0x710000678	25-7	2	2	1	0x7100008c8	30	0
927	207		0x710000678	25-7	2	3	1	0x7100008c8	30	1
928	208	Tr_m2(4)	0x710000680	26-0	2	2	1	0x7100008d0	2	0
929	208		0x710000680	26-0	2	3	1	0x7100008d0	2	1
930	209	Tr_m2(5)	0x710000688	26-1	2	2	1	0x7100008d0	6	0
931	209		0x710000688	26-1	2	3	1	0x7100008d0	6	1
932	210	Tr_m2(6)	0x710000690	26-2	2	2	1	0x7100008d0	10	0
933	210		0x710000690	26-2	2	3	1	0x7100008d0	10	1
934	211	Tr_m2(7)	0x710000698	26-3	2	2	1	0x7100008d0	14	0

935	211		0x710000698	26-3	2	3	1	0x7100008d0	14	1
936	212	Tr_m2(8)	0x7100006a0	26-4	2	2	1	0x7100008d0	18	0
937	212		0x7100006a0	26-4	2	3	1	0x7100008d0	18	1
938	213	Tr_m2(9)	0x7100006a8	26-5	2	2	1	0x7100008d0	22	0
939	213		0x7100006a8	26-5	2	3	1	0x7100008d0	22	1
940	214	Tr_m2(10)	0x7100006b0	26-6	2	2	1	0x7100008d0	26	0
941	214		0x7100006b0	26-6	2	3	1	0x7100008d0	26	1
942	215	Tr_m2(11)	0x7100006b8	26-7	2	2	1	0x7100008d0	30	0
943	215		0x7100006b8	26-7	2	3	1	0x7100008d0	30	1
944	216	Tr_m2(12)	0x7100006c0	27-0	2	2	1	0x7100008d8	2	0
945	216		0x7100006c0	27-0	2	3	1	0x7100008d8	2	1
946	217	Tr_m2(13)	0x7100006c8	27-1	2	2	1	0x7100008d8	6	0
947	217		0x7100006c8	27-1	2	3	1	0x7100008d8	6	1
948	218	Tr_m2(14)	0x7100006d0	27-2	2	2	1	0x7100008d8	10	0
949	218		0x7100006d0	27-2	2	3	1	0x7100008d8	10	1
950	219	Tr_m2(15)	0x7100006d8	27-3	2	2	1	0x7100008d8	14	0
951	219		0x7100006d8	27-3	2	3	1	0x7100008d8	14	1
952	220	Tr_m2(16)	0x7100006e0	27-4	2	2	1	0x7100008d8	18	0
953	220		0x7100006e0	27-4	2	3	1	0x7100008d8	18	1
954	221	Tr_m2(17)	0x7100006e8	27-5	2	2	1	0x7100008d8	22	0
955	221		0x7100006e8	27-5	2	3	1	0x7100008d8	22	1
956	222	Tr_m2(18)	0x7100006f0	27-6	2	2	1	0x7100008d8	26	0
957	222		0x7100006f0	27-6	2	3	1	0x7100008d8	26	1
958	223		0x7100006f8	27-7	2	2	1	0x7100008d8	30	0
959	223		0x7100006f8	27-7	2	3	1	0x7100008d8	30	1

Event description

This chapter lists meaning of each event, groped by the unit name. For each event, a counter number which is used to count this event is given. To each event, only one counter is assigned. For configuration needed to select each event, use the counter number to locate it in the previous table and to read out the associated configuration register, and values which have to be selected. All configuration registers come out of reset cleared, so writing zeros is not necessary.

450 & FPU

Signal name	Name	Counter	Description
Dp0-pp0(0) Dp1_pp0(0) Dp0-pp1(0) Dp1_pp1(0)	C450_XXXEJPIPEINSTR	0, 0, 35, 35	Number of J-pipe instruction
Dp0-pp0(1) Dp1_pp0(1) Dp0-pp1(1) Dp1_pp1(1)	C450_XXXEJPIPEINTFAST	1 1 36 36	PowerPC Add/Sub in J-pipe
Dp0-pp0(2) Dp1_pp0(2) Dp0-pp1(2) Dp1_pp1(2)	C450_XXXEJPIPELOGICAL	2 2 37 37	PowerPC logical operations in J-pipe
Dp0-pp0(3) Dp1_pp0(3) Dp0-pp1(3) Dp1_pp1(3)	C450_XXXEJPIPESHROTMK	3 3 38 38	shift/rotate/mask instructions
Dp0-pp0(4) Dp1_pp0(4) Dp0-pp1(4) Dp1_pp1(4)	C450_XXXEIPIPEINSTR	4 4 39 39	Number of I-pipe instruction
Dp0-pp0(5) Dp1_pp0(5) Dp0-pp1(5) Dp1_pp1(5)	C450_XXXEIPIPEINTSLOW	5 5 40 40	PowerPC Mul/Div in I-pipe
Dp0-pp0(6) Dp1_pp0(6) Dp0-pp1(6) Dp1_pp1(6)	C450_XXXEIPIPEINTFAST	6 6 41 41	PowerPC Add/Sub in I-pipe
Dp0-pp0(7) Dp1_pp0(7) Dp0-pp1(7) Dp1_pp1(7)	C450_XXXEIPIPELOGICAL	7 7 42 42	PowerPC logical operations in I-pipe
Dp0-pp0(8) Dp1_pp0(8) Dp0-pp1(8) Dp1_pp1(8)	C450_XXXEIPIPESHROTMK	8 8 43 43	shift/rotate/mask instructions
Dp0-pp0(9) Dp1_pp0(9) Dp0-pp1(9) Dp1_pp1(9)	C450_XXXEIPIPEBRANCH	9 9 44 44	PowerPC branches
Dp0-pp0(10) Dp1_pp0(10) Dp0-pp1(10) Dp1_pp1(10)	C450_XXXEIPIPETLBOP	10 10 45 45	PowerPC TLB operations
Dp0-pp0(11) Dp1_pp0(11) Dp0-pp1(11) Dp1_pp1(11)	C450_XXXEIPIPEPROCCTL	11 11 46 46	PowerPC process control
Dp0-pp0(12) Dp1_pp0(12) Dp0-pp1(12) Dp1_pp1(12)	C450_XXXEIPIPEOTHER	12 12 47 47	PowerPC other I-pipe operations

Dp0-pp0(13) Dp1_pp0(13) Dp0-pp1(13) Dp1_pp1(13)	C450_XXXDLINEFILLINPROG	13 13 48 48	No. of cycles D-cache LineFillInProgress
Dp0-pp0(14) Dp1_pp0(14) Dp0-pp1(14) Dp1_pp1(14)	C450_XXXILINEFILLINPROG	14 14 49 49	No. of cycles I-cache LineFillInProgress
Dp0-pp0(15) Dp1_pp0(15) Dp0-pp1(15) Dp1_pp1(15)	C450_XXXDCACHEMISS	15 15 50 50	Accesses to D cache which miss in D Cache
Dp0-pp0(16) Dp1_pp0(16) Dp0-pp1(16) Dp1_pp1(16)	C450_XXXDCACHEHIT	16 16 51 51	Accesses to D cache which hit in D Cache
Dp0-pp0(17) Dp1_pp0(17) Dp0-pp1(17) Dp1_pp1(17)	C450_XXXDINSTRUCTLOAD	17 17 52 52	PowerPC data loads
Dp0-pp0(18) Dp1_pp0(18) Dp0-pp1(18) Dp1_pp1(18)	C450_XXXDINSTRUCTSTORE	18 18 53 53	PowerPC data stores
Dp0-pp0(19) Dp1_pp0(19) Dp0-pp1(19) Dp1_pp1(19)	C450_XXXDINSTRUCTCACH EOP	19 19 54 54	
Dp0-pp0(20) Dp1_pp0(20) Dp0-pp1(20) Dp1_pp1(20)	C450_XXXICACHEMISS	20 20 55 55	Accesses to I cache which miss in I Cache
Dp0-pp0(21) Dp1_pp0(21) Dp0-pp1(21) Dp1_pp1(21)	C450_XXXICHCHEHIT	21 21 56 56	Accesses to I cache which hit in I Cache
Dp0-pp0(22) Dp1_pp0(22) Dp0-pp1(22) Dp1_pp1(22)	FPUPERFMON(0)	22 22 57 57	PowerPC FP Add/Sub `Fadd, fadds, fsub, fsubs`

Dp0-pp0(23)
Dp1_pp0(23)
Dp0-pp1(23)
Dp1_pp1(23)
	FPUPERFMON(1)	23
		23
		58
		58
			PowerPC FP Mult
			`fmul`
			`fmuls`

Dp0-pp0(24)
Dp1_pp0(24)
Dp0-pp1(24)
Dp1_pp1(24)
	FPUPERFMON(2)	24
		24
		59
		59
			`PowerPC FP FMA`
			`Fmadd, fmadds, fmsub, fmsubs, fnmadd`
			`fnmadds, fnmsub, fnmsubs`
			1 result generated per instruction, 2 flops

Dp0-pp0(25)
Dp1_pp0(25)
Dp0-pp1(25)
Dp1_pp1(25)
	FPUPERFMON(3)	25
		25
		60
		60
			`PowerPC FP Div`
			`Fdiv, fdivs`
			Single Pipe Divide

Dp0-pp0(26) Dp1_pp0(26) Dp0-pp1(26) Dp1_pp1(26)	FPUPERFMON(4)	26 26 61 61	PowerPC FP remaining non-storage instructions fabs, fnabs, frsp, fctiw, fctiw, fctiwz, fres, frsqrte, fsel, fmr fneg, fcmpu, fcmpo, mffs, mcrfs, mtfsfi, mtfsf, mtfsb0, mtfsb1
Dp0-pp0(27) Dp1_pp0(27) Dp0-pp1(27) Dp1_pp1(27)	FPUPERFMON(5)	27 27 62 62	Dual pipe Add/Sub fpadd fpsub
Dp0-pp0(28) Dp1_pp0(28) Dp0-pp1(28) Dp1_pp1(28)	FPUPERFMON(6)	28 28 63 63	Dual pipe Mult Fpmul, fxmul, fxpmul, fxsmul
Dp0-pp0(29) Dp1_pp0(29) Dp0-pp1(29) Dp1_pp1(29)	FPUPERFMON(7)	29 29 64 64	Dual pipe FMA's Fpmadd, fpnmadd, fpmsub, fpnmsub fxmadd, fxnmadd, fxmsub, fxnmsub fxcpmadd, fxcsmadd, fxcpnmadd fxcsnmadd, fxcpmsub, fxcsmsub fxcpnmsub, fxcsnmsub, fxcpnpma fxcsnpma, fxcpnsma, fxcsnsma fxcxnpma, fxcxnsma, fxcxma fxcxnms 2 results generated per instruction, 4 flops
Dp0-pp0(30) Dp1_pp0(30) Dp0-pp1(30) Dp1_pp1(30)	FPUPERFMON(8)	30 30 65 65	Dual pipe remaining non-storage instructions Fpmr, fpneg, fsmr, fsneg, fxmr Fsmfp, fsmtp, fpabs, fpnabs Fsabs, fsnabs, fprsp, fpctiw Fpctiwz, fpre, fprsqrte, fpsel fscmp
Dp0-pp0(31) Dp1_pp0(31) Dp0-pp1(31) Dp1_pp1(31)	FPUPERFMON(9)	31 31 66 66	Quad Word Loads Lfpdx, lfpdux, lfxdx, lfxdux
Dp0-pp0(32) Dp1_pp0(32) Dp0-pp1(32) Dp1_pp1(32)	FPUPERFMON(10)	32 32 67 67	All other Loads Lfs, lfsx, lfsu, lfsux, lfpsx, fpsux, lfsdx, lfsdux, lfssx, lfssux, lfd, lfdx, lfdu, lfdux, lfxsx, Lfxsux
Dp0-pp0(33) Dp1_pp0(33) Dp0-pp1(33) Dp1_pp1(33)	FPUPERFMON(11)	33 33 68 68	Quad Word Stores Stfpdx, stfpdux, stfxdx, stfxdux
Dp0-pp0(34) Dp1_pp0(34) Dp0-pp1(34) Dp1_pp1(34)	FPUPERFMON(12)	34 34 69 69	All other FPU Stores Stfs, stfsx, stfsu, stfsux, stfd, stfdx, stfdu, stfdux, stfiwx, stfpsx, stfpsux, stfpiwx, stfsdx, stfsdux, stfssx,stfssux, stfxsx, stfxsux

Snoop filters

Signal	Name	CD	Trigger	Counter	Description	Mode
Dp0-snp0(0) Dp0-snp1(0) Dp1-snp0(0) Dp1-snp1(0)	INVREQ	x1	Level high	70 71 70 71	L1 invalidation requested	0 0 1 1
Dp0-snp0(1) Dp0-snp1(1) Dp1-snp0(1) Dp1-snp1(1)	SNPREQ0	x2	Level high	176 185 236 245	Port 0 received a snoop request from a remote source	0 0 1 1
Dp0-snp0(2) Dp0-snp1(2) Dp1-snp0(2) Dp1-snp1(2)	SNPREQ1	x2	Level high	177 186 237 246	Port 1 received a snoop request from a remote source	0 0 1 1
Dp0-snp0(3) Dp0-snp1(3) Dp1-snp0(3) Dp1-snp1(3)	SNPREQ2	x2	Level high	178 187 238 247	Port 2 received a snoop request from a remote source	0 0 1 1
Dp0-snp0(4) Dp0-snp1(4) Dp1-snp0(4) Dp1-snp1(4)	SNPREQ3	x2	Level high	179 188 239 248	Port 3 received a snoop request from a remote source	0 0 1 1
Dp0-snp0(5) Dp0-snp1(5) Dp1-snp0(5) Dp1-snp1(5)	SFHIT0	x2	Level high	180 189 240 249	Port 0 snoop filter rejected a snoop request	0 0 1 1
Dp0-snp0(6) Dp0-snp1(6) Dp1-snp0(6) Dp1-snp1(6)	SFHIT1	x2	Level high	181 190 241 250	Port 1 snoop filter rejected a snoop request	0 0 1 1
Dp0-snp0(7) Dp0-snp1(7) Dp1-snp0(7) Dp1-snp1(7)	SFHIT2	x2	Level high	182 191 242 251	Port 2 snoop filter rejected a snoop request	0 0 1 1
Dp0-snp0(8) Dp0-snp1(8) Dp1-snp0(8) Dp1-snp1(8)	SFHIT3	x2	Level high	183 192 243 252	Port 3 snoop filter rejected a snoop request	0 0 1 1
Dp0-snp0(9) Dp0-snp1(9) Dp1-snp0(9) Dp1-snp1(9)	WRAP	x2	Level high	184 193 244 253	Snoop filter detected an L1 cache wrap	0 0 1 1
Dp0-snp0(10) Dp0-snp1(10) Dp1-snp0(10) Dp1-snp1(10)	SCHIT0	x2	Level high	72 100 147 175	Port 0 snoop cache rejected a request	2 2 3 3
Dp0-snp0(11) Dp0-snp1(11) Dp1-snp0(11) Dp1-snp1(11)	SCHIT1	x2	Level high	73 101 148 176	Port 1 snoop cache rejected a request	2 2 3 3
Dp0-snp0(12) Dp0-snp1(12) Dp1-snp0(12)	SCHIT2	x2	Level high	74 102 149	Port 2 snoop cache rejected a request	2 2 3

Dp1-snp1(12)				177		3
Dp0-snp0(13) Dp0-snp1(13) Dp1-snp0(13) Dp1-snp1(13)	SCHIT3	x2	Level high	75 103 150 178	Port 3 snoop cache rejected a request	2 2 3 3
Dp0-snp0(14) Dp0-snp1(14) Dp1-snp0(14) Dp1-snp1(14)	SRAHIT0	x2	Level high	76 104 151 179	Port 0 request hit a stream register in the active set	2 2 3 3
Dp0-snp0(15) Dp0-snp1(15) Dp1-snp0(15) Dp1-snp1(15)	SRAHIT1	x2	Level high	77 105 152 180	Port 1 request hit a stream register in the active set	2 2 3 3
Dp0-snp0(16) Dp0-snp1(16) Dp1-snp0(16) Dp1-snp1(16)	SRAHIT2	x2	Level high	78 106 153 181	Port 2 request hit a stream register in the active set	2 2 3 3
Dp0-snp0(17) Dp0-snp1(17) Dp1-snp0(17) Dp1-snp1(17)	SRAHIT3	x2	Level high	79 107 154 182	Port 3 request hit a stream register in the active set	2 2 3 3
Dp0-snp0(18) Dp0-snp1(18) Dp1-snp0(18) Dp1-snp1(18)	SRHHIT0	x2	Level high	80 108 155 183	Port 0 request hit a stream register in the history set	2 2 3 3
Dp0-snp0(19) Dp0-snp1(19) Dp1-snp0(19) Dp1-snp1(19)	SRHHIT1	x2	Level high	81 109 156 184	Port 1 request hit a stream register in the history set	2 2 3 3
Dp0-snp0(20) Dp0-snp1(20) Dp1-snp0(20) Dp1-snp1(20)	SRHHIT2	x2	Level high	82 110 157 185	Port 2 request hit a stream register in the history set	2 2 3 3
Dp0-snp0(21) Dp0-snp1(21) Dp1-snp0(21) Dp1-snp1(21)	SRHHIT3	x2	Level high	83 111 158 186	Port 3 request hit a stream register in the history set	2 2 3 3
Dp0-snp0(22) Dp0-snp1(22) Dp1-snp0(22) Dp1-snp1(22)	SRMIS0	x2	Level high	84 112 159 187	Port 0 stream register rejected a request	2 2 3 3
Dp0-snp0(23) Dp0-snp1(23) Dp1-snp0(23) Dp1-snp1(23)	SRMIS1	x2	Level high	85 113 160 188	Port 1 stream register rejected a request	2 2 3 3
Dp0-snp0(24) Dp0-snp1(24) Dp1-snp0(24) Dp1-snp1(24)	SRMIS2	x2	Level high	86 114 161 189	Port 2 stream register rejected a request	2 2 3 3
Dp0-snp0(25) Dp0-snp1(25) Dp1-snp0(25) Dp1-snp1(25)	SRMIS3	x2	Level high	87 115 162 190	Port 3 stream register rejected a request	2 2 3 3
Dp0-snp0(26) Dp0-snp1(26)	RFHIT0	x2	Level high	88 116	Port 0 range filter rejected a request	2 2

Dp1-snp0(26) Dp1-snp1(26)				163 191		3 3
Dp0-snp0(27) Dp0-snp1(27) Dp1-snp0(27) Dp1-snp1(27)	RFHIT1	x2	Level high	89 117\ 164 192	Port 1 range filter rejected a request	2 2 3 3
Dp0-snp0(28) Dp0-snp1(28) Dp1-snp0(28) Dp1-snp1(28)	RFHIT2	x2	Level high	90 118 165 193	Port 2 range filter rejected a request	2 2 3 3
Dp0-snp0(29) Dp0-snp1(29) Dp1-snp0(29) Dp1-snp1(29)	RFHIT3	x2	Level high	91 119 166 194	Port 3 range filter rejected a request	2 2 3 3
Dp0-snp0(30) Dp0-snp1(30) Dp1-snp0(30) Dp1-snp1(30)	SCU0	x2	Level high	92 120 167 195	Port 0 snoop cache updated cache line	2 2 3 3
Dp0-snp0(31) Dp0-snp1(31) Dp1-snp0(31) Dp1-snp1(31)	SCU1	x2	Level high	93 121 168 196	Port 1 snoop cache updated cache line	2 2 3 3
Dp0-snp0(32) Dp0-snp1(32) Dp1-snp0(32) Dp1-snp1(32)	SCU2	x2	Level high	94 122 169 197	Port 2 snoop cache updated cache line	2 2 3 3
Dp0-snp0(33) Dp0-snp1(33) Dp1-snp0(33) Dp1-snp1(33)	SCU3	x2	Level high	95 123 170 198	Port 3 snoop cache updated cache line	2 2 3 3
Dp0-snp0(34) Dp0-snp1(34) Dp1-snp0(34) Dp1-snp1(34)	SCR0	x2	Level high	96 124 171 199	Port 0 snoop filtered by both snoop cache and filter registers	2 2 3 3
Dp0-snp0(35) Dp0-snp1(35) Dp1-snp0(35) Dp1-snp1(35)	SCR1	x2	Level high	97 125 172 200	Port 1 snoop filtered by both snoop cache and filter registers	2 2 3 3
Dp0-snp0(36) Dp0-snp1(36) Dp1-snp0(36) Dp1-snp1(36)	SCR2	x2	Level high	98 126 173 201	Port 2 snoop filtered by both snoop cache and filter registers	2 2 3 3
Dp0-snp0(37) Dp0-snp1(37) Dp1-snp0(37) Dp1-snp1(37)	SCR3	x2	Level high	99 127 174 202	Port 3 snoop filtered by both snoop cache and filter registers	2 2 3 3

L2

Signal		Counter	Description	Trigger	Mode
Dp0_l20(0)		72	Prefetch request valid	Level high	0
Dp0_l21(0)		104			0
Dp1_l20(0)		132			1
Dp1_l21(0)		164			1
Dp0_l20(1)		73	Prefetch hits in filter	Level high	0
Dp0_l21(1)		105			0
Dp1_l20(1)		133			1
Dp1_l21(1)		165			1
Dp0_l20(2)		74	Prefetch hits in active stream	Level high	0
Dp0_l21(2)		106			0
Dp1_l20(2)		134			1
Dp1_l21(2)		166			1
Dp0_l20(3)		75	Number of cycles for which L2-prefetch is pending	Level high	0
Dp0_l21(3)		107			0
Dp1_l20(3)		135			1
Dp1_l21(3)		167			1
Dp0_l20(4)		76	requested PF is already in L2	Level high	0
Dp0_l21(4)		108			0
Dp1_l20(4)		136			1
Dp1_l21(4)		168			1
Dp0_l20(5)		77	Prefetch snoop hit from same core (write)	Level high	0
Dp0_l21(5)		109			0
Dp1_l20(5)		137			1
Dp1_l21(5)		169			1
Dp0_l20(6)		78	Prefetch snoop hit from other core	Level high	0
Dp0_l21(6)		110			0
Dp1_l20(6)		138			1
Dp1_l21(6)		170			1
Dp0_l20(7)		79	Prefetch snoop hit PLB (write)	Level high	0
Dp0_l21(7)		111			0
Dp1_l20(7)		139			1
Dp1_l21(7)		171			1
Dp0_l20(8)		80	number of cycles for which read request is pending	Level high	0
Dp0_l21(8)		112			0
Dp1_l20(8)		140			1
Dp1_l21(8)		172			1
Dp0_l20(9)		81	read requests	Level high	0
Dp0_l21(9)		113			0
Dp1_l20(9)		141			1
Dp1_l21(9)		173			1
Dp0_l20(10)		82	devbus read requests (for SRAM, LOCK & UPC)	Level high	0
Dp0_l21(10)		114			0
Dp1_l20(10)		142			1
Dp1_l21(10)		174			1
Dp0_l20(11)		83	L3 read request	Level high	0
Dp0_l21(11)		115			0
Dp1_l20(11)		143			1
Dp1_l21(11)		175			1
Dp0_l20(12)		84	netbus read requests (for tree & torus)	Level high	0
Dp0_l21(12)		116			0

Dp1_l20(12)		144			1
Dp1_l21(12)		176			1
Dp0_l20(13)		85	BLIND device read request	Level high	0
Dp0_l21(13)		117			0
Dp1_l20(13)		145			1
Dp1_l21(13)		177			1
Dp0_l20(14)		86	prefetchable requests	Level high	0
Dp0_l21(14)		118			0
Dp1_l20(14)		146			1
Dp1_l21(14)		178			1
Dp0_l20(15)		87	L2 hit	Level high	0
Dp0_l21(15)		119			0
Dp1_l20(15)		147			1
Dp1_l21(15)		178			1
Dp0_l20(16)		88	same core snoops	Level high	0
Dp0_l21(16)		120			0
Dp1_l20(16)		148			1
Dp1_l21(16)		179			1
Dp0_l20(17)		89	other core snops	Level high	0
Dp0_l21(17)		121			0
Dp1_l20(17)		149			1
Dp1_l21(17)		180			1
Dp0_l20(18)		90	other DP PU0 snoops	Level high	0
Dp0_l21(18)		122			0
Dp1_l20(18)		150			1
Dp1_l21(18)		181			1
Dp0_l20(19)		91	other DP PU1 snoops	Level high	0
Dp0_l21(19)		123			0
Dp1_l20(19)		151			1
Dp1_l21(19)		182			1
Dp0_l20(20)		92	reserved		
Dp0_l21(20)		124			
Dp1_l20(20)		152			
Dp1_l21(20)		183			
Dp0_l20(21)		93	reserved		
Dp0_l21(21)		125			
Dp1_l20(21)		153			
Dp1_l21(21)		184			
Dp0_l20(22)		94	reserved		
Dp0_l21(22)		126			
Dp1_l20(22)		154			
Dp1_l21(22)		185			
Dp0_l20(23)		95	reserved		
Dp0_l21(23)		127			
Dp1_l20(23)		155			
Dp1_l21(23)		186			
Dp0_l20(24)		96	reserved		
Dp0_l21(24)		128			
Dp1_l20(24)		156			
Dp1_l21(24)		187			
Dp0_l20(25)		97	reserved		
Dp0_l21(25)		129			
Dp1_l20(25)		157			
Dp1_l21(25)		188			
Dp0_l20(26)		98	reserved		

Dp0_l21(26) Dp1_l20(26) Dp1_l21(26)		130 158 189			
Dp0_l20(27) Dp0_l21(27) Dp1_l20(27) Dp1_l21(27)		99 131 159 190	reserved		
Dp0_l20(28) Dp0_l21(28) Dp1_l20(28) Dp1_l21(28)		100 132 160 191	reserved		
Dp0_l20(29) Dp0_l21(29) Dp1_l20(29) Dp1_l21(29)		101 133 161 192	Number of writes to L3	Level low	0 0 1 1
Dp0_l20(30) Dp0_l21(30) Dp1_l20(30) Dp1_l21(30)		102 134 162 193	Number of writes to network	Level low	0 0 1 1
Dp0_l20(31) Dp0_l21(31) Dp1_l20(31) Dp1_l21(31)		103 135 163 194	Number of writes to devbus	Level high	0 0 1 1

L3

Signal		Counter	Description	Trigger	Mode
L30_m0(0) L31_m0(0)		136 156	Rd 0: single line delivered to L2	Level high	0 0
L30_m0(1) L31_m0(1)		137 157	Rd 0: burst delivered to L2	Level high	0 0
L30_m0(2) L31_m0(2)		138 158	Rd 0: read return collision	Level high	0 0
L30_m0(3) L31_m0(3)		139 159	Rd 0: dir0 hit or in flight	Level high	0 0
L30_m0(4) L31_m0(4)		140 160	Rd 0: dir0 miss or lock-down	Level high	0 0
L30_m0(5) L31_m0(5)		141 161	Rd 0: dir1 hit or in flight	Level high	0 0
L30_m0(6) L31_m0(6)		142 162	Rd 0: dir1 miss or lock-down	Level high	0 0
L30_m0(7) L31_m0(7)		143 163	Rd 1: single line delivered to L2	Level high	0 0
L30_m0(8) L31_m0(8)		144 164	Rd 1: burst delivered to L2	Level high	0 0
L30_m0(9) L31_m0(9)		145 165	Rd 1: read return collision	Level high	0 0
L30_m0(10) L31_m0(10)		146 166	Rd 1: dir0 hit or in flight	Level high	0 0
L30_m0(11) L31_m0(11)		147 167	Rd 1: dir0 miss or lock-down	Level high	0 0
L30_m0(12) L31_m0(12)		148 168	Rd 1: dir1 hit or in flight	Level high	0 0
L30_m0(13) L31_m0(13)		149 169	Rd 1: dir1 miss or lock-down	Level high	0 0
L30_m0(14) L31_m0(14)		150 170	Dir 0: number of lookups	Level high	0 0
L30_m0(15) L31_m0(15)		151 171	Dir 0: number of cycles with requests that are not taken	Level high	0 0
L30_m0(16) L31_m0(16)		152 172	Dir 1: number of lookups	Level high	0 0
L30_m0(17) L31_m0(17)		153 173	Dir 1: number of cycles with requests that are not taken	Level high	0 0
L30_m0(18) L31_m0(18)		154 174	M0-18/MH: number of stores to DDR	Level high	0 0
L30_m0(19) L31_m0(19)		155 175	M0-19/MH: number of fetches from DDR	Level high	0 0
L30_m1(0) L31_m1(0)		196 216	Rd 2: single line delivered to L2	Level high	1 1
L30_m1(1) L31_m1(1)		197 217	Rd 2: burst delivered to L2	Level high	1 1
L30_m1(2) L31_m1(2)		198 218	Rd 2: read return collision	Level high	1 1
L30_m1(3) L31_m1(3)		199 219	Rd 2: dir0 hit or in flight	Level high	1 1
L30_m1(4) L31_m1(4)		200 220	Rd 2: dir0 miss or lock-down	Level high	1 1

L30_m1(5) L31_m1(5)		201 221	Rd 2: dir1 hit or in flight	Level high	1 1
L30_m1(6) L31_m1(6)		202 222	Rd 2: dir1 miss or lock-down	Level high	1 1
L30_m1(7) L31_m1(7)		203 223	WRB 0: total accepted deposit requests from write queues to write buffer	Level high	1 1
L30_m1(8) L31_m1(8)		204 224	WRB 0: number of cycles with requests from queues that are not taken	Level high	1 1
L30_m1(9) L31_m1(9)		205 225	WRB 1: total accepted deposit requests from write queues to write buffer	Level high	1 1
L30_m1(10) L31_m1(10)		206 226	WRB 1: number of cycles with requests from queues that are not taken	Level high	1 1
L30_m1(11) L31_m1(11)		207 227	MH: number of allocation requests to write buffer	Level high	1 1
L30_m1(12) L31_m1(12)		208 228	MH: number of allocation request cycles to writebuffer without being taken	Level high	1 1
L30_m1(13) L31_m1(13)		209 229	PF: number of line prefetches brought into eDRAM	Level high	1 1
L30_m1(14) L31_m1(14)		210 230	reserved		
L30_m1(15) L31_m1(15)		211 231	reserved		
L30_m1(16) L31_m1(16)		212 232	reserved		
L30_m1(17) L31_m1(17)		213 233	reserved		
L30_m1(18) L31_m1(18)		214 234	reserved		
L30_m1(19) L31_m1(19)		215 235	reserved		

Torus

Signal	Name	Counter	Description	Trigger	Mode
Td_torus(0)	xp packets	194	No. of packets sent to X+ dimension	Level high	0
Td_torus(1)	xp 32 B chunks	195	No. of 32B chunks sent to X+	Level high	0
Td_torus(2)	xm packets	196	No. of packets sent to X- dimension	Level high	0
Td_torus(3)	xm 32 B chunks	197	No. of 32B chunks sent to X-	Level high	0
Td_torus(4)	yp packets	198	No. of packets sent to Y+ dimension	Level high	0
Td_torus(5)	yp 32 B chunks	199	No. of 32B chunks sent to Y+	Level high	0
Td_torus(6)	ym packets	200	No. of packets sent to Y- dimension	Level high	0
Td_torus(7)	ym 32 B chunks	201	No. of 32B chunks sent to Y-	Level high	0
Td_torus(8)	zp packets	202	No. of packets sent to Z+ dimension	Level high	0
Td_torus(9)	zp 32 B chunks	203	No. of 32B chunks sent to Z+	Level high	0
Td_torus(10)	zm packets	204	No. of packets sent to Z- dimension	Level high	0
Td_torus(11)	zm 32 B chunks	205	No. of 32B chunks sent to Z-	Level high	0
Td_torus(12)	xp token/acks	128	No. of protocol token/ack packets in xp	Level high	2
Td_torus(13)	xp acks	129	No. of protocol ack packets in xp	Level high	2
Td_torus(14)	xp vcd0 chunks	130	No. of 32B chunks sent on dynamic vc 0	Level high	2
Td_torus(15)	xp vcd1 chunks	131	No. of 32B chunks sent on dynamic vc 1	Level high	2
Td_torus(16)	xp vcbn chunks	132	No. of 32B chunks sent on bubble vc 2	Level high	2
Td_torus(17)	xp vcbp chunks	133	No. of 32B chunks sent on priority vc 3	Level high	2
Td_torus(18)	xp no tokens	134	xp link avail, no vcd0 vcd1 tokens	Level high	2
Td_torus(19)	xp no vcd0 tokens	135	xp link avail; no vcd0 vcd; vcbn tokens	Level high	2
Td_torus(20)	no vcbn tokens	136	xp link avail; no vcbn tokens	Level high	2
Td_torus(21)	no vcbp tokens	137	xp link avail; no vcbp tokens	Level high	2
Td_torus(22)	xm token/acks	138	No. of protocol token/ack packets in xm	Level high	2
Td_torus(23)	xm acks	139	No. of protocol ack packets in xm	Level high	2
Td_torus(24)	xm vcd0 chunks	140	No. of 32B chunks sent on dynamic vc 0	Level high	2
Td_torus(25)	xm vcd1 chunks	141	No. of 32B chunks sent on dynamic vc 1	Level high	2
Td_torus(26)	xm vcbn chunks	142	No. of 32B chunks sent on bubble vc 2	Level high	2
Td_torus(27)	xm vcbp chunks	143	No. of 32B chunks sent on priority vc 3	Level high	2
Td_torus(28)	xm no tokens	144	xm link avail; no vcd0 vcd1 tokens	Level high	2
Td_torus(29)	xm no vcd0 tokens	145	xm link avail; no vcd0 vcd; vcbn tokens	Level high	2
Td_torus(30)	xm no vcbn tokens	146	xm link avail; no vcbn tokens	Level high	2
Td_torus(31)	xm no vcbp tokens	147	xm link avail; no vcbp tokens	Level high	2
Td_torus(32)	yp token/acks	148	No. of protocol token/ack packets in yp	Level high	2
Td_torus(33)	yp acks	149	No. of protocol ack packets in yp	Level high	2
Td_torus(34)	yp vcd0 chunks	150	No. of 32B chunks sent on dynamic vc 0	Level high	2
Td_torus(35)	yp vcd1 chunks	151	No. of 32B chunks sent on dynamic vc 1	Level high	2
Td_torus(36)	yp vcbn chunks	152	No. of 32B chunks sent on bubble vc 2	Level high	2
Td_torus(37)	yp vcbp chunks	153	No. of 32B chunks sent on priority vc 3	Level high	2
Td_torus(38)	yp no tokens	154	yp link avail; no vcd0 vcd1tokens	Level high	2
Td_torus(39)	yp no vcd0 tokens	155	yp link avail; no vcd0 vcd; vcbn tokens	Level high	2
Td_torus(40)	yp no vcbn tokens	156	yp link avail; no vcbn tokens	Level high	2
Td_torus(41)	yp no vcbp tokens	157	yp link avail; no vcbp tokens	Level high	2
Td_torus(42)	ym token/acks	158	No. of protocol token/ack packets in ym	Level high	2
Td_torus(43)	ym acks	159	No. of protocol ack packets in ym	Level high	2
Td_torus(44)	ym vcd0 chunks	160	No. of 32B chunks sent on dynamic vc 0	Level high	2
Td_torus(45)	ym vcd1 chunks	161	No. of 32B chunks sent on dynamic vc 1	Level high	2
Td_torus(46)	ym vcbn chunks	162	No. of 32B chunks sent on bubble vc 2	Level high	2
Td_torus(47)	ym vcbp chunks	163	No. of 32B chunks sent on priority vc 3	Level high	2
Td_torus(48)	ym no tokens	164	ym link avail; no vcd0 vcd1 tokens	Level high	2
Td_torus(49)	ym no vcd0 tokens	165	ym link avail; no vcd0 vcd; vcbn tokens	Level high	2

Td_torus(50)	ym no vcbn tokens	166	ym link avail; no vcbn tokens	Level high	2
Td_torus(51)	ym no vcbp tokens	167	ym link avail; no vcbp tokens	Level high	2
Td_torus(52)	zp token/acks	168	No. of protocol token/ack packets in zp	Level high	2
Td_torus(53)	zp acks	169	No. of protocol ack packets in zp	Level high	2
Td_torus(54)	zp vcd0 chunks	170	No. of 32B chunks sent on dynamic vc 0	Level high	2
Td_torus(55)	zp vcd1 chunks	171	No. of 32B chunks sent on dynamic vc 1	Level high	2
Td_torus(56)	zp vcbn chunks	172	No. of 32B chunks sent on bubble vc 2	Level high	2
Td_torus(57)	zp vcbp chunks	173	No. of 32B chunks sent on priority vc 3	Level high	2
Td_torus(58)	zp no tokens	174	zp link avail; no vcd0 vcd1 tokens	Level high	2
Td_torus(59)	zp no vcd0 tokens	175	zp link avail; no vcd0 vcd; vcbn tokens	Level high	2
Td_torus(60)	zp no vcbn tokens	176	zp link avail; no vcbn tokens	Level high	2
Td_torus(61)	zp no vcbp tokens	177	zp link avail; no vcbp tokens	Level high	2
Td_torus(62)	zm token/acks	178	No. of protocol token/ack packets in zm	Level high	2
Td_torus(63)	zm acks	179	No. of protocol ack packets in zm	Level high	2
Td_torus(64)	zm vcd0 chunks	180	No. of 32B chunks sent on dynamic vc 0	Level high	2
Td_torus(65)	zm vcd1 chunks	181	No. of 32B chunks sent on dynamic vc 1	Level high	2
Td_torus(66)	zm vcbn chunks	182	No. of 32B chunks sent on bubble vc 2	Level high	2
Td_torus(67)	zm vcbp chunks	183	No. of 32B chunks sent on priority vc 3	Level high	2
Td_torus(68)	zm no tokens	184	zm link avail; no vcd0 vcd1 tokens	Level high	2
Td_torus(69)	zm no vcd0 tokens	185	zm link avail; no vcd0 vcd; vcbn tokens	Level high	2
Td_torus(70)	zm no vcbn tokens	186	zm link avail; no vcbn tokens	Level high	2
Td_torus(71)	zm no vcbp tokens	187	zm link avail; no vcbp tokens	Level high	2

DMA

Signal	Name	Counter	Description	Trigger	
Td_dma(0)	N pkt inj	206	Number of packets injected	Level high	Mode
Td_dma(1)	N desc read	207	Number of descriptors read from L3	Level high	0
Td_dma(2)	N fifo pkt recv	208	Number of fifo packets received	Level high	0
Td_dma(3)	N cntr pkt recv	209	Number of counter packets received	Level high	0
Td_dma(4)	N rget pkt recv	210	Number of remote get packets received	Level high	0
Td_dma(5)	N L3 rd req	211	Number of read requests to L3 by IDPU	Level high	0
Td_dma(6)	N L3 rd valid	212	Number of read valid returned from L3	Level high	0
Td_dma(7)	N L3 rd ack	213	Number of DMA L3 read requests acknowledged by the L3	Level high	0
Td_dma(8)	N L3 wr active	214	Number of cycles rdpu wants to write to L3, independent of the write ready	Level high	0
Td_dma(9)	N L3 wr req	215	Number of write requests to L3	Level high	0
Td_dma(10)		216	reserved		
Td_dma(11)		217	reserved		
Td_dma(12)		218	reserved		
Td_dma(13)		219	reserved		
Td_dma(14)		220	reserved		
Td_dma(15)		221	reserved		
Td_dma(16)		188	reserved		
Td_dma(17)		189	reserved		
Td_dma(18)		190	reserved		
Td_dma(19)		191	reserved		
Td_dma(20)		192	reserved		
Td_dma(21)		193	reserved		
Td_dma(22)		194	reserved		
Td_dma(23)		195	reserved		
Td_dma(24)		196	reserved		
Td_dma(25)		197	reserved		
Td_dma(26)		198	reserved		
Td_dma(27)		199	reserved		
Td_dma(28)		200	reserved		
Td_dma(29)		201	reserved		
Td_dma(30)		202	reserved		
Td_dma(31)		203	reserved		

Collective

Signal	Name	Counter	Description	Trigger	Mode
Tr_m0(0)		222	arbiter_core ch2_vc0_mature	Level high	0
Tr_m0(1)		223	arbiter_core ch1_vc0_mature	Level high	0
Tr_m0(2)		224	arbiter_core ch0_vc0_mature	Level high	0
Tr_m0(3)		225	arbiter_core inj_vc0_mature	Level high	0
Tr_m0(4)		226	arbiter_core ch2_vc1_mature	Level high	0
Tr_m0(5)		227	arbiter_core ch1_vc1_mature	Level high	0
Tr_m0(6)		228	arbiter_core ch0_vc1_mature	Level high	0
Tr_m0(7)		229	arbiter_core inj_vc1_mature	Level high	0
Tr_m0(8)		230	arbiter_core requests pending	Level high	0
Tr_m0(9)		231	arbiter_core requests waiting (ready to go)	Level high	0
Tr_m0(10)		232	Arbiter receiver 2 packet taken	Level high	0
Tr_m0(11)		233	Arbiter receiver 1 packet taken	Level high	0
Tr_m0(12)		234	Arbiter receiver 0 packet taken	Level high	0
Tr_m0(13)		235	Arbiter local client packet taken	Level high	0
Tr_m0(14)		236	Receiver 0 vc0 data packet received	Level high	0
Tr_m0(15)		237	Receiver 0 vc1 data packet received	Level high	0
Tr_m0(16)		238	Receiver 1 vc0 data packet received	Level high	0
Tr_m0(17)		239	Receiver 1 vc1 data packet received	Level high	0
Tr_m0(18)		240	Receiver 2 vc0 data packet received	Level high	0
Tr_m0(19)		241	Receiver 2 vc1 data packet received	Level high	0
Tr_m0(20)		242	Sender 0 vc0 DATA packets sent	Level high	0
Tr_m0(21)		243	Sender 0 vc1 DATA packets sent	Level high	0
Tr_m0(22)		244	Sender 1 vc0 DATA packets sent	Level high	0
Tr_m0(23)		245	Sender 1 vc1 DATA packets sent	Level high	0
Tr_m0(24)		246	Sender 2 vc0 DATA packets sent	Level high	0
Tr_m0(25)		247	Sender 2 vc1 DATA packets sent	Level high	0
Tr_m0(26)		248	Injection vc0 header	Level high	0
Tr_m0(27)		249	Injection vc1 header added	Level high	0
Tr_m0(28)		250	Reception vc0 packet added	Level high	0
Tr_m0(29)		251	Reception vc1 packet added	Level high	0
Tr_m1(0)		72	arbiter_core ch2_vc0_mature	Level high	1
Tr_m1(1)		73	arbiter_core ch1_vc0_mature	Level high	1
Tr_m1(2)		74	arbiter_core ch0_vc0_mature	Level high	1
Tr_m1(3)		75	arbiter_core inj_vc0_mature	Level high	1
Tr_m1(4)		76	arbiter_core ch2_vc1_mature	Level high	1
Tr_m1(5)		77	arbiter_core ch1_vc1_mature	Level high	1
Tr_m1(6)		78	arbiter_core ch0_vc1_mature	Level high	1
Tr_m1(7)		79	arbiter_core inj_vc1_mature	Level high	1
Tr_m1(8)		80	Receiver 0 vc0 empty packet	Level high	1
Tr_m1(9)		81	Receiver 0 vc1 empty packet	Level high	1

Tr_m1(10)		82	Receiver 0 IDLE packet	Level high	1
Tr_m1(11)		83	Receiver 0 known-bad-packet marker	Level high	1
Tr_m1(12)		84	Receiver 0 vc0 cut-through	Level high	1
Tr_m1(13)		85	Receiver 0 vc1 cut-through	Level high	1
Tr_m1(14)		86	Receiver 0 header parity error	Level high	1
Tr_m1(15)		87	Receiver 0 unexpected header error	Level high	1
Tr_m1(16)		88	Receiver 0 resynch-mode (after error)	Level high	1
Tr_m1(17)		89	Receiver 1 vc0 empty packet	Level high	1
Tr_m1(18)		90	Receiver 1 vc1 empty packet	Level high	1
Tr_m1(19)		91	Receiver 1 IDLE packet	Level high	1
Tr_m1(20)		92	Receiver 1 known-bad-packet marker	Level high	1
Tr_m1(21)		93	Receiver 1 vc0 cut-through	Level high	1
Tr_m1(22)		94	Receiver 1 vc1 cut-through	Level high	1
Tr_m1(23)		95	Receiver 1 header parity error	Level high	1
Tr_m1(24)		96	Receiver 1 unexpected header error	Level high	1
Tr_m1(25)		97	Receiver 1 resynch-mode (after error)	Level high	1
Tr_m1(26)		98	Receiver 2 vc0 empty packet	Level high	1
Tr_m1(27)		99	Receiver 2 vc1 empty packet	Level high	1
Tr_m1(28)		100	Receiver 2 IDLE packet	Level high	1
Tr_m1(29)		101	Receiver 2 known-bad-packet marker	Level high	1
Tr_m1(30)		102	Receiver 2 vc0 cut-through	Level high	1
Tr_m1(31)		103	Receiver 2 vc1 cut-through	Level high	1
Tr_m1(32)		104	Receiver 2 header parity error	Level high	1
Tr_m1(33)		105	Receiver 2 unexpected header error	Level high	1
Tr_m1(34)		106	Receiver 2 resynch-mode (after error)	Level high	1
Tr_m1(35)		107	Sender 0 vc0 cut-through	Level high	1
Tr_m1(36)		108	Sender 0 vc1 cut-through	Level high	1
Tr_m1(37)		109	Sender 0 vc0 packet sent (total)	Level high	1
Tr_m1(38)		110	Sender 0 vc1 packet sent (total)	Level high	1
Tr_m1(39)		111	Sender 0 IDLE packets sent	Level high	1
Tr_m1(40)		112	Sender 1 vc0 cut-through	Level high	1
Tr_m1(41)		113	Sender 1 vc1 cut-through	Level high	1
Tr_m1(42)		114	Sender 1 vc0 packet sent (total)	Level high	1
Tr_m1(43)		115	Sender 1 vc1 packet sent (total)	Level high	1
Tr_m1(44)		116	Sender 1 IDLE packets sent	Level high	1
Tr_m1(45)		117	Sender 2 vc0 cut-through	Level high	1
Tr_m1(46)		118	Sender 2 vc1 cut-through	Level high	1
Tr_m1(47)		119	Sender 2 vc0 packet sent (total)	Level high	1
Tr_m1(48)		120	Sender 2 vc1 packet sent (total)	Level high	1
Tr_m1(49)		121	Sender 2 IDLE packets sent	Level high	1
Tr_m1(50)		122	Injection vc0 payload added	Level high	1
Tr_m1(51)		123	Injection vc1 payload added	Level high	1
Tr_m1(52)		124	Injection vc0 packet taken	Level high	1
Tr_m1(53)		125	Injection vc1 packet taken	Level high	1
Tr_m1(54)		126	Reception vc0 header taken	Level high	1
Tr_m1(55)		127	Reception vc1 header taken	Level high	1
Tr_m1(56)		128	Reception vc0 payload taken	Level high	1
Tr_m1(57)		129	Reception vc1 payload taken	Level high	1

Tr_m1(58)		130	Reception vc0 packet discarded	Level high	1
Tr_m1(59)		131	Reception vc1 packet discarded	Level high	1
Tr_m2(0)		204	Arbiter receiver 2 abort	Level high	2
Tr_m2(1)		205	Arbiter receiver 1 abort	Level high	2
Tr_m2(2)		206	Arbiter receiver 0 abort	Level high	2
Tr_m2(3)		207	Arbiter local client abort	Level high	2
Tr_m2(4)		208	Receiver 0 vc0 full	Level high	2
Tr_m2(5)		209	Receiver 0 vc1 full	Level high	2
Tr_m2(6)		210	Receiver 1 vc0 full	Level high	2
Tr_m2(7)		211	Receiver 1 vc1 full	Level high	2
Tr_m2(8)		212	Receiver 2 vc0 full	Level high	2
Tr_m2(9)		213	Receiver 2 vc1 full	Level high	2
Tr_m2(10)		214	Sender 0 vc0 empty	Level high	2
Tr_m2(11)		215	Sender 0 vc1 empty	Level high	2
Tr_m2(12)		216	Sender 0 resend attempts	Level high	2
Tr_m2(13)		217	Sender 1 vc0 empty	Level high	2
Tr_m2(14)		218	Sender 1 vc1 empty	Level high	2
Tr_m2(15)		219	Sender 1 resend attempts	Level high	2
Tr_m2(16)		220	Sender 2 vc0 empty	Level high	2
Tr_m2(17)		221	Sender 2 vc1 empty	Level high	2
Tr_m2(18)		222	Sender 2 resend attempts	Level high	2
Tr_m3(0)		72	Arbiter ch2_vc0_have	Level high	2
Tr_m3(1)		73	Arbiter ch1_vc0_have	Level high	2
Tr_m3(2)		74	Arbiter ch0_vc0_have	Level high	2
Tr_m3(3)		75	Arbiter inj_vc0_have	Level high	2
Tr_m3(4)		76	Arbiter ch2_vc1_have	Level high	2
Tr_m3(5)		77	Arbiter ch1_vc1_have	Level high	2
Tr_m3(6)		78	Arbiter ch0_vc1_have	Level high	2
Tr_m3(7)		79	Arbiter inj_vc1_have	Level high	2
Tr_m3(8)		80	arbiter_core greedy_mode	Level high	3
Tr_m3(9)		81	arbiter_core requests pending	Level high	3
Tr_m3(10)		82	arbiter_core requests waiting (ready to go)	Level high	3
Tr_m3(11)		83	Arbiter class 0 wins	Level high	3
Tr_m3(12)		84	Arbiter class 1 wins	Level high	3
Tr_m3(13)		85	Arbiter class 2 wins	Level high	3
Tr_m3(14)		86	Arbiter class 3 wins	Level high	3
Tr_m3(15)		87	Arbiter class 4 wins	Level high	3
Tr_m3(16)		88	Arbiter class 5 wins	Level high	3
Tr_m3(17)		89	Arbiter class 6 wins	Level high	3
Tr_m3(18)		90	Arbiter class 7 wins	Level high	3
Tr_m3(19)		91	Arbiter class 8 wins	Level high	3
Tr_m3(20)		92	Arbiter class 9 wins	Level high	3
Tr_m3(21)		93	Arbiter class 10 wins	Level high	3
Tr_m3(22)		94	Arbiter class 11 wins	Level high	3
Tr_m3(23)		95	Arbiter class 12 wins	Level high	3
Tr_m3(24)		96	Arbiter class 13 wins	Level high	3
Tr_m3(25)		97	Arbiter class 14 wins	Level high	3
Tr_m3(26)		98	Arbiter class 15 wins	Level high	3
Tr_m3(27)		99	Arbiter sender 2 busy	Level high	3
Tr_m3(28)		100	Arbiter sender 1 busy	Level high	3
Tr_m3(29)		101	Arbiter sender 0 busy	Level high	3
Tr_m3(30)		102	Arbiter local client busy (reception)	Level high	3
Tr_m3(31)		103	Arbiter receiver 2 busy	Level high	3

Tr_m3(32)		104	Arbiter receiver 1 busy	Level high	3
Tr_m3(33)		105	Arbiter receiver 0 busy	Level high	3
Tr_m3(34)		106	Arbiter local client busy (injection)	Level high	3
Tr_m3(35)		107	Arbiter ALU busy	Level high	3
Tr_m3(36)		108	Arbiter receiver 2 abort	Level high	3
Tr_m3(37)		109	Arbiter receiver 1 abort	Level high	3
Tr_m3(38)		110	Arbiter receiver 0 abort	Level high	3
Tr_m3(39)		111	Arbiter local client abort	Level high	3
Tr_m3(40)		112	Arbiter receiver 2 packet taken	Level high	3
Tr_m3(41)		113	Arbiter receiver 1 packet taken	Level high	3
Tr_m3(42)		114	Arbiter receiver 0 packet taken	Level high	3
Tr_m3(43)		115	Arbiter local client packet taken	Level high	3
Tr_m3(44)		116	Receiver 0 vc0 data packet received	Level high	3
Tr_m3(45)		117	Receiver 0 vc1 data packet received	Level high	3
Tr_m3(46)		118	Receiver 0 vc1 full	Level high	3
Tr_m3(47)		119	Receiver 0 header parity error	Level high	3
Tr_m3(48)		120	Receiver 1 vc0 data packet received	Level high	3
Tr_m3(49)		121	Receiver 1 vc1 data packet received	Level high	3
Tr_m3(50)		122	Receiver 1 vc0 full	Level high	3
Tr_m3(51)		123	Receiver 1 vc1 full	Level high	3
Tr_m3(52)		124	Receiver 2 vc0 data packet received	Level high	3
Tr_m3(53)		125	Receiver 2 vc1 data packet received	Level high	3
Tr_m3(54)		126	Receiver 2 vc0 full	Level high	3
Tr_m3(55)		127	Receiver 2 vc1 full	Level high	3
Tr_m3(56)		128	Sender 0 vc0 empty	Level high	3
Tr_m3(57)		129	Sender 0 vc1 empty	Level high	3
Tr_m3(58)		130	Sender 0 vc0 DATA packets sent	Level high	3
Tr_m3(59)		131	Sender 0 vc1 DATA packets sent	Level high	3
Tr_m3(60)		132	Sender 0 resend attempts	Level high	3
Tr_m3(61)		133	Sender 1 vc0 empty	Level high	3
Tr_m3(62)		134	Sender 1 vc1 empty	Level high	3
Tr_m3(63)		135	Sender 1 vc0 DATA packets sent	Level high	3
Tr_m3(64)		136	Sender 1 vc1 DATA packets sent	Level high	3
Tr_m3(65)		137	Sender 1 resend attempts	Level high	3
Tr_m3(66)		138	Sender 2 vc0 empty	Level high	3
Tr_m3(67)		139	Sender 2 vc1 empty	Level high	3
Tr_m3(68)		140	Sender 2 vc0 DATA packets sent	Level high	3
Tr_m3(69)		141	Sender 2 vc1 DATA packets sent	Level high	3
Tr_m3(70)		142	Sender 2 resend attempts	Level high	3
Tr_m3(71)		143	Injection vc0 header added	Level high	3
Tr_m3(72)		144	Injection vc1 header added	Level high	3
Tr_m3(73)		145	Reception vc0 packet added	Level high	3
Tr_m3(74)		146	Reception vc1 packet added	Level high	3